

n-channel JFETs designed for . . .



U320 U321 U322

Performance Curves NIP
See Section 5

- VHF Buffer Amplifiers
- IF Amplifiers

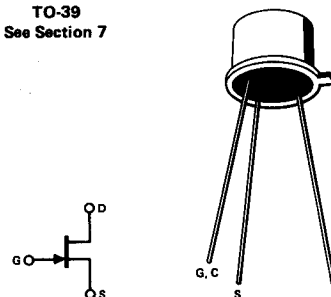
BENEFITS

- High Gain
 $g_{fs} = 120,000 \mu\text{mho Typical}$
- Wide Dynamic Range
- Low Intermodulation Distortion

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	100 mA
Total Device Dissipation (25°C Case Temperature)	3 W
Power Derating (to 150°C)	24 mW/°C
Storage Temperature Range	-55 to +150°C
Operating Temperature Range	-55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-39
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

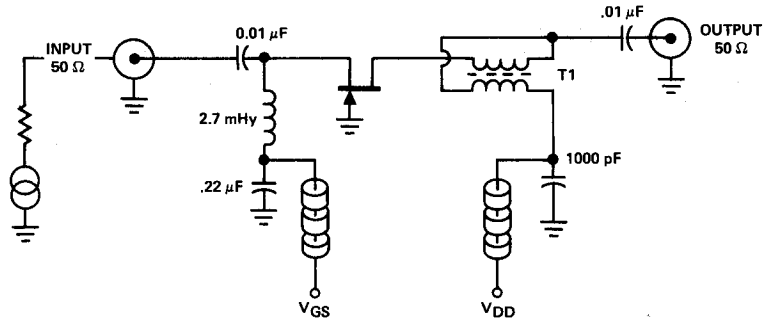
Characteristic	U320			U321			U322			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 I _{GSS} Gate Reverse Current (Note 1)			-3			-3			-3	nA	V _{GS} = -15 V, V _{DS} = 0 V
2 V _{GS(off)} Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	μA	T = 100°C
3 BV _{GSS} Gate-Source Breakdown Voltage	-25			-25			-25			V	V _{DS} = 5 V, I _D = 1 mA
4 I _{DSS} Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	I _G = -1 μA, V _{DS} = 0 V
5 V _{GS(f)} Gate-Source Forward Voltage			1			1			1	V	I _G = 1 mA, V _{DS} = 0 V
6 r _{DS(on)} Drain-Source ON Resistance			10			11			8	Ω	V _{GS} = 0 V, I _D = 10 mA
7 g _{fs} Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V _{DS} = 15 V, V _{GS} = 0 V
8 C _{iss} Common-Source Input Capacitance			30			30			30	pF	V _{GS} = -10 V, V _{DS} = 0 V f = 1 MHz
9 C _{rss} Common-Source Reverse Transfer Capacitance			15			15			15	pF	
10 C _{gs} Gate-Source Capacitance		12			12			12		pF	
11 C _{gd} Gate-Drain Capacitance		12			12			12		pF	V _{GS} = -10 V, I _D = 0 V _{GD} = -10 V, I _S = 0
12 e _n Equivalent Short Circuit Input Noise Voltage		2			2			2		nV/√Hz	V _{DS} = 5 V, I _D = 10 mA
13 g _{fg} Common Gate Forward Transconductance		55			55			55		mmho	V _{DG} = 20 V, I _D = 25 mA
14 g _{ig} Common-Gate Input Conductance		56			56			56		mmho	
15 g _{og} Common-Gate Output Conductance		0.5			0.5			0.5		mmho	
16 G _{PS} Power Gain (Note 3)		9			9			9		dB	V _{DS} = 15 V, V _{GS} = 0 V
17 F _T Gain-Bandwidth (Note 4)		400			400			400		MHz	
18 NF Noise Figure (Note 3)		2.5			2.5			2.5		dB	V _{DG} = 20 V, I _D = 25 mA
19 NF Noise Figure (Note 3)		2.5			2.5			2.5		dB	V _{DG} = 20 V, I _D = 25 mA

- NOTES:**
- Approximately doubles for every 10°C increase in T_A.
 - Pulse test duration = 2 ms.
 - Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
 - Computed as g_{fs}/C_{rss}.

NIP

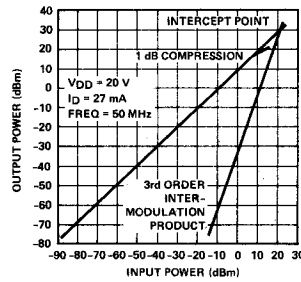
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Siliconix



T1-6 TURNS #22 AWG TWISTED PAIR WIRE ON 0.375 INCH DIAMETER INDIANA GENERAL F625-9Q2 TOROID CORE.

50 MHz Power Gain and Noise Figure Test Circuit for U320, U321 and U322
Figure 1



Gain - Intermodulation Characteristics
Figure 2