SP9770B & C

10-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9770 is an ECL 10K compatible 10-bit DAC. The 12nsec settling time allows a 75 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9770 design includes a high performance voltage reference and reference amplifier.

FEATURES

- Operating Temperature Range -30°C to +85°C
- 12ns Settling Time 1 LSB Typically
- **SP9770B** 10 Bits ±½ LSB Integral and ±½ LSB Differential Linearity
- **SP9770C** 10 Bits ±½ LSB Integral and ±1 LSB Differential Linearity
- Current Output
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

ORDERING INFORMATION

SP9770B DC (Industrial - Sidebrazed DILMON package)
SP9770C DC (Industrial - Sidebrazed DILMON package)
SP9770BB DC (Plessey High Reliability Ceramic DIL package)

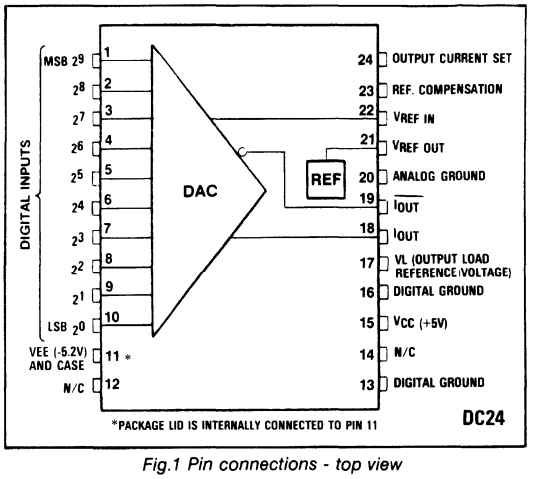

Fig.1 Pin connections - top view

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems

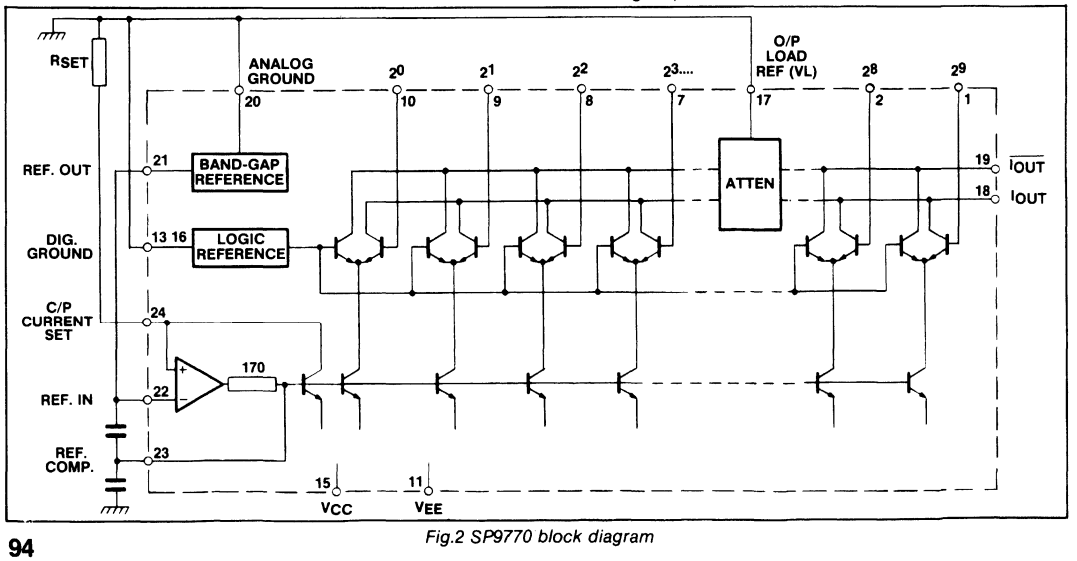

Fig.2 SP9770 block diagram

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V	Output reference supply (V_L)	0 to +3V
Negative supply voltage	-5.7V	Reference input	±2V
Digital input voltage	0 to -4.5V	Storage temperature range	-65°C to +150°C
Minimum R_{SET} (from 0V)	175Ω	Junction operating temperature	<175°C
Maximum R_{SET}	2.5kΩ	Lead temperature (soldering 60 sec)	300°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C; V_{CC} = +5.00V ± 5%; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{CC}	7.0	12.0	17.0	mA	All inputs at
Supply current I_{EE}	45.0	56.0	70.0	mA	-1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	μA	All inputs HI
Reference voltage V_{REF}	-1.250	-1.280	-1.300	V	
Reference voltage temp. coeff.		40	80	ppm/°C	-30°C to +85°C
Output current - full scale	2		30	mA	R_{SET} 2.5kΩ - 175Ω
Output current - full scale	20.2	21.3	22.4	mA	R_{SET} = 240Ω
Output compliance	-1.0		+1.0	V	T_{amb} =25°C See
	-0.7		+1.0	V	T_{amb} =85°C Note 4
Bit size (LSB)	19.7	20.8	21.9	μA	Current output
Resolution	10			Bits	
	0.098			%	
Differential non-linearity			0.5	LSB	
Integral non-linearity			0.5	LSB	SP9770B
			1.0	LSB	SP9770C
Output dynamic parameters (see Note 1)					
Rise time		2.0	3.0	ns	10 to 90%
Settling time - full scale		12	20	ns	To 1 LSB
Glitch energy		90	150	psV	Mid-point
Glitch duration			4	ns	transition
Noise output		-90	-83	dBm	See Note 2
Multiplying mode - voltage (see Fig.5)					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		200		kHz	-3dB see Note 3
Transfer function non-linearity		0.2	1.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 23). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.

Thermal characteristics θ_{JA} = 65°C/W
θ_{JC} = 15°C/W

APPLICATION

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} \triangleq 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

RECOMMENDATIONS

For low output noise it is best to use a chip capacitor on pin 23 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended.

For low glitch output it is essential that the input time skew and ringing is minimised. The Plessey SP9210 is a suitable high speed latch for this purpose.

Eurocard construction is not recommended.

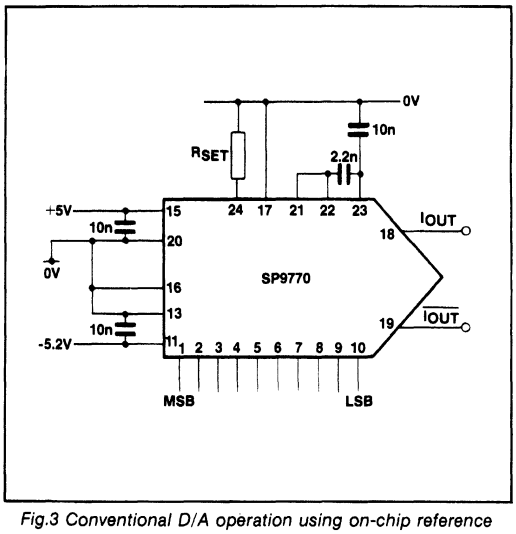

Fig.3 Conventional D/A operation using on-chip reference

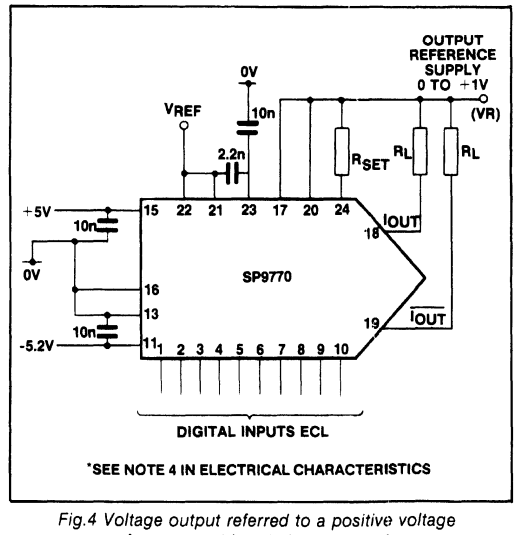

Fig.4 Voltage output referred to a positive voltage for outputs biased above ground

OPERATING NOTES

Output Compliance

Fig.4 shows the method of using the SP9770 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pins 17 and 20, and the current setting resistor R_{SET} to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause slight degradation of linearity.

Voltage multiplying. A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

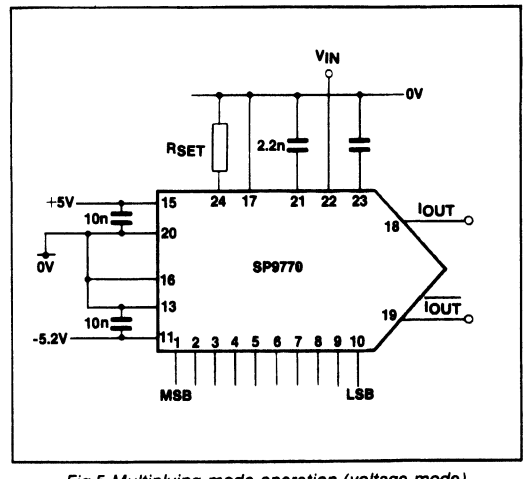

Fig.5 Multiplying mode operation (voltage mode)