Consumer Microcircuits Limited

PRODUCT INFORMATION

FX609 Continuously Variable Slope Delta Modulation (CVSD) Codec

Publication D/609/3 March 1988
Provisional Issue

Features

- Full Duplex CVSD Codec
- On-Chip Input and Output Filters
- Selectable 3 or 4-Bit Compand Algorithm
- Programmable Sampling Clocks
- Forced Idle Facility
- Powersave Facility
- Low Power 5V CMOS

Applications

- Digital Speech Communications
- Time Domain Scramblers
- Digital Cordless Telephone
- Voice Storage
- Digital Delay Lines
- Speech Analysis
- Multiplexers
- General Purpose

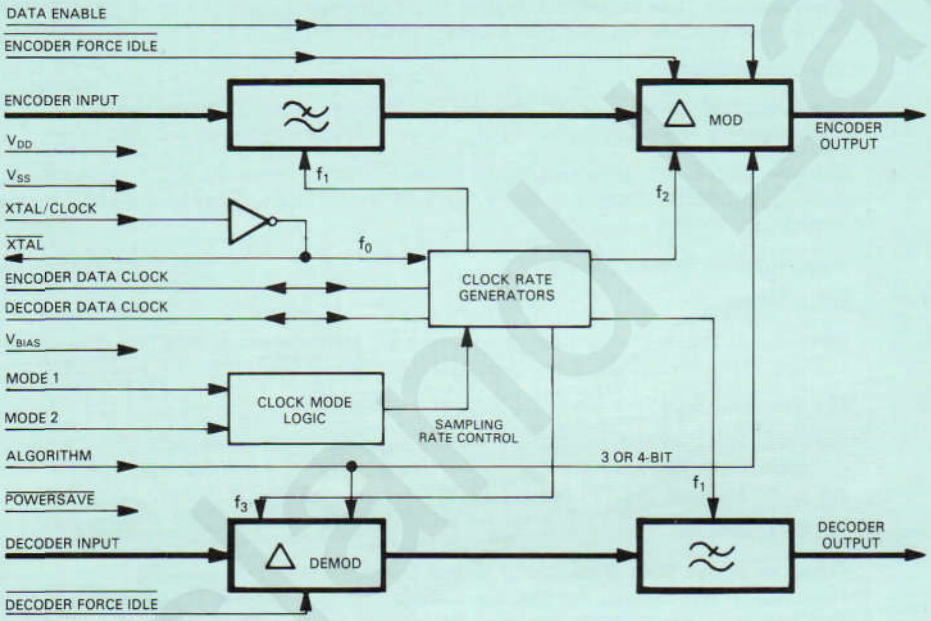


Fig. 1 Internal Block Diagram

FX609

Brief Description

The FX609 is an LSI circuit designed as a Continuously Variable Slope Delta Modulation (CVSD) Codec and is intended for use in voice storage, time domain speech scramblers and digital speech communications equipment. Encode input and decoder output analogue filters are incorporated on-chip and use switched capacitor technology. Sampling clock rates can be programmed to 16, 32 or 64k bits/second from an internal clock generator or may be externally applied in the range 8 to 64k bits/second. Sampling clock frequencies are output for the synchronisation of external circuits. The internal clocks are derived from an on-chip reference oscillator using an externally connected crystal. The encoder has an enable function for use in multiplexer applications. When not enabled, the encoder output is high impedance (three-state). Forced idle facilities in the encoder cause a perfect 1010....output pattern and in the decoder an output voltage of $V_{DD}/2$. The companding circuits may be operated with a 3 or 4-bit algorithm which is externally selected. The device may be put into standby mode by selection of the powersave facility. The FX609 is a low power, 5 volt CMOS device and is available in 22- pin DIL, 24-pin plastic quad or 28-pin PLCC packages.

Pin Number			Function
DIL FX609J	Quad Plastic FX609LG	PLCC FX609LH	
1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A nominal 1.024MHz xtal input or externally derived clock is injected here. See Fig. 2.
	2	2	**No connection.**
2	3	3	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
3	4	4	**No Connection.**
4	5	5	**Encoder Data Clock:** A Logic I/O port. External encode clock input or internal data clock output. Clock frequency dependent upon clock mode 1, 2 inputs and xtal frequency (see **Clock Mode** pins).
5	6	6	**Encoder Output:** The encoder digital output, this is a three state output:
		7, 8	**No Connection.**
6	7	9	**Encoder Force Idle:** When this pin is at logical '0' the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup.
7	8	10	**Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup.
8	9	11	**No Connection.**
9	10	12	**Bias:** Normally at $V_{DD}/2$ bias, this pin requires to be externally decoupled by a capacitor, C_2. Internally pulled to V_{SS} when "$\overline{\text{Powersave}}$" is logical '0'.
10	11	13	**Encoder Input:** The analogue signal input. Internally biased at $V_{DD}/2$, an external 1μF input coupling capacitor, C_1, is required on this input. See Fig. 2 Note 3 for source impedance details.
11	12	14	V_{SS}: Negative Supply (GND).
12	13	15,16	**No connection.**
13	14	17	**Decoder Output:** The recovered analogue signal is output at this pin, it is the buffered output of a low pass filter. During "$\overline{\text{Powersave}}$" this output is o/c.
14	15	18,19	**No Connection.**
15	16	20	**$\overline{\text{Powersave}}$:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.
	17	21	**No Connection.**
16	18	22	**$\overline{\text{Decoder Force Idle}}$:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.
17	19	23	**Decoder Input:** Received digital signal input. Internal 1MΩ Pullup.
18	20	24	**Decoder Data Clock:** A Logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1, 2 inputs, see **Clock Mode** pins.
19	21	25	**Algorithm:** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.
20	22	26	**Clock Mode 2:** These inputs select encoder and decoder data clock modes.
21	23	27	**Clock Mode 1:**
22	24	28	V_{DD}: **Positive Supply:** A single +5 volt power supply is required.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	V_{SS}

Internal 1MΩ pull-ups.

Clock 1	Mode 2	
0	0	External Clocks
0	1	Internal, 64kb/s = f ÷ 16
1	0	Internal, 32kb/s = f ÷ 32
1	1	Internal, 16kb/s = f ÷ 64

Clock rates refer to f = 1.024MHz Xtal/Clock input.
During Internal Data Clock operation the data clock frequencies are available at the ports for external circuit synchronisation. Independent or Common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

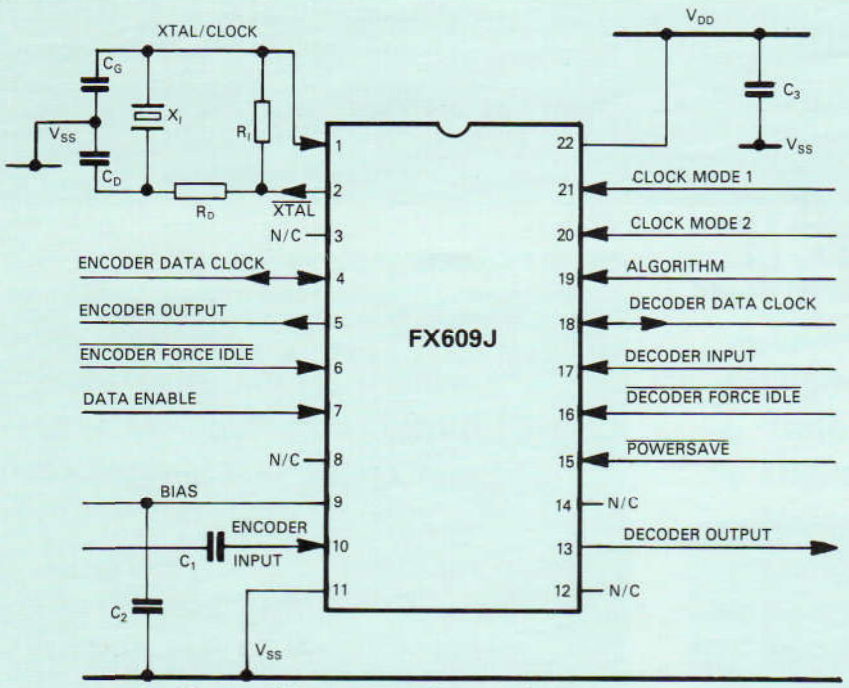


Fig. 2 External Component Connections

Component References		
Component	Unit Value	Note
R_1	Typ. 1 M	1
R_D	Selectable	1
C_1	1.0μ	
C_2	1.0μ	
C_3	1.0μ	
C_D	Typ. 33p	1
C_G	Typ. 68p	1
X_1	1.024 MHz	1, 2

Tolerance

Resistors ±10%
Capacitors ±20%

NOTES

1. *Xtal circuitry shown is in accordance with CML application note D/XT/1 April '86.*
2. *A 1.024 MHz clock/xtal input will yield exactly 16/32/64 kb/s data clock rates.*
3. *To prevent unwanted internal oscillations at the encoder input pin, the source impedance to this input must be less than 100Ω. Output noise levels will improve with even lower source impedances.*

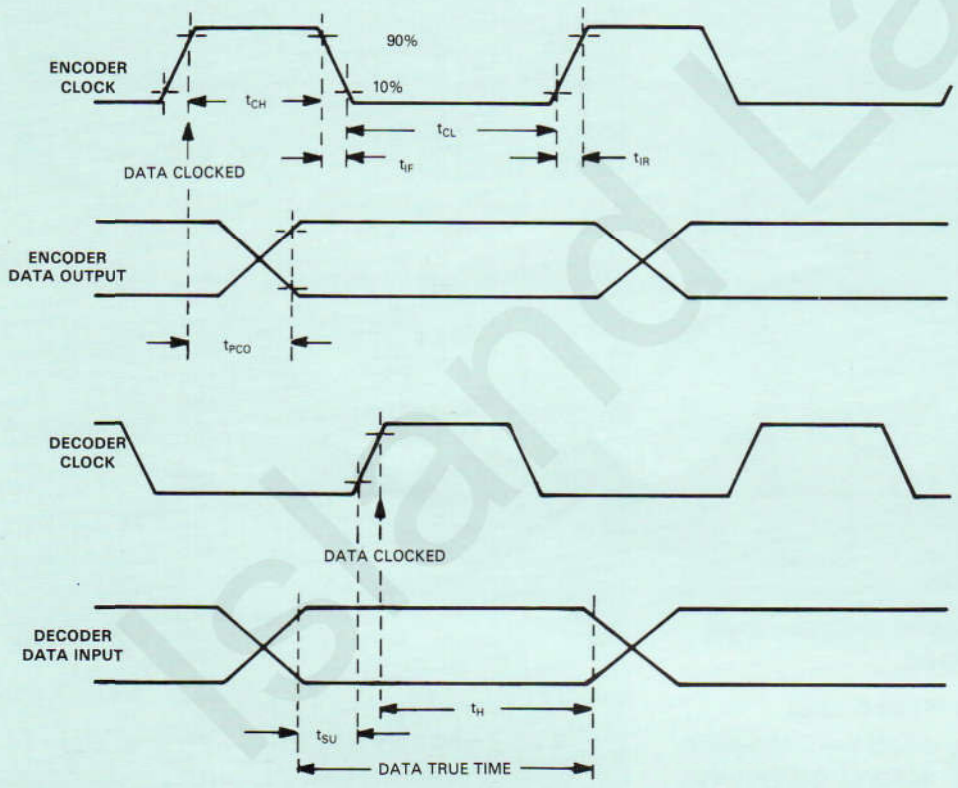


Fig. 3 Codec Timing Diagrams

TIMING

t_{CH} *Clock '1' Pulse Widths 1μs Min.*

t_{CL} *Clock '0' Pulse Widths 1μs Min.*

t_{IR} *Clock Rise Time 100ns Typ.*

t_{IF} *Clock Fall Time 100ns Typ.*

t_{SU} *Data Set-up Time 450ns Max.*

t_H *Data Hold Time 600ns Min.*

$t_{SU} + t_H$ *Data True Time*

t_{PCO} *Clock to Output Delay Time = 750ns Max. Xtal input 1.024 MHz.*

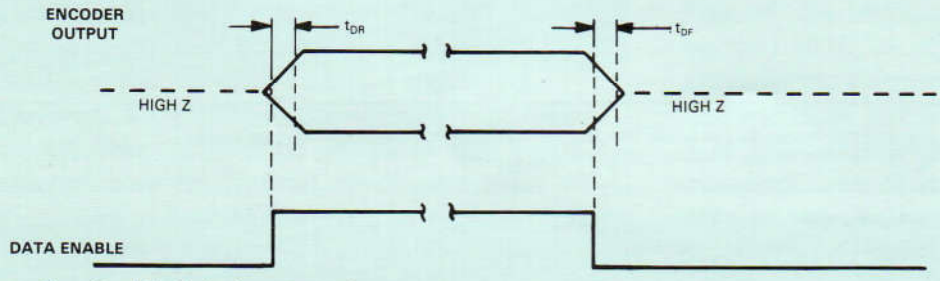


Fig. 4 Multiplexing Function

TIMING

t_{DR} *Data Rise Time 100ns Typ.*

t_{DF} *Data Fall Time 100ns Typ.*

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3 to (V_{DD} + 0.3V)
Output sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX609J**	−30°C to +85°C (Ceramic)
	FX609LG/LH	−30°C to +70°C (Plastic)
Storage temperature range:	**FX609J**	−55°C to +125°C (Ceramic)
	FX609LG/LH	−40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5V, T_{amb} = 25°C, Xtal/Clock (f) = 1.024 MHz, Sample Rate 32kb/s.
[Standard Test Signal 820Hz, ref. 0dB = 489mV (rms)]

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		—	3.5	—	mA
Supply Current (Powersave)		—	500	—	µA
Inputs Logic '1'		3.5	—	—	V
Inputs Logic '0'		—	—	1.5	V
Outputs Logic '1'		4.0	—	—	V
Outputs Logic '0'		—	—	1.0	V
Digital Input Impedance (logic I/O pins)		—	10	—	MΩ
Digital Input Impedance (logic input pins, pullup resistor)	2	300	—	—	kΩ
Digital Output Impedance		—	4	—	kΩ
Analogue Input Impedance		—	100	—	kΩ
Analogue Output Impedance		—	800	—	Ω
Three State Output leakage Current (output disabled)		—	±4	—	µA
Insertion Loss		—	0	—	dB
Dynamic Values	1				
Encoder:					
Analogue Signal Input levels	5	−30	—	+8	dB
Principal Integrator Frequency		—	275	—	Hz
Encoder Passband			3400		Hz
Compand Time Constant		—	4	—	ms
Decoder:					
Analogue Signal Output levels	5	−30	—	+8	dB
Decoder Passband		300	—	3400	Hz
Encoder Decoder (Full codec):					
Passband		300	—	3400	Hz
Stopband		6	—	10	kHz
Stopband Attenuation		—	60	—	dB
Passband Gain		—	0	—	dB
Passband Ripple		−3	—	+3	dB
Output Noise (Input short circuit)		—	−60	—	dB
Perfect Idle Channel Noise (Encode Forced)		—	−63	—	dB
Group Delay Distortion	3				
1000 − 2600Hz		—	—	450	µs
600 − 2800Hz		—	—	750	µs
500 − 3000Hz		—	—	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

Notes:
1. *Dynamic characteristics specified at 5V only.*
2. *All logic Inputs except, Encoder and Decoder Data Clocks.*
3. *Group delay distortion for full codec relative to the delay at 820Hz, −20dB at the encoder input.*
4. *Relative timings are shown on Figures 3 and 4.*
5. *Recommended values—see graph Fig. 7.*

Codec Performance

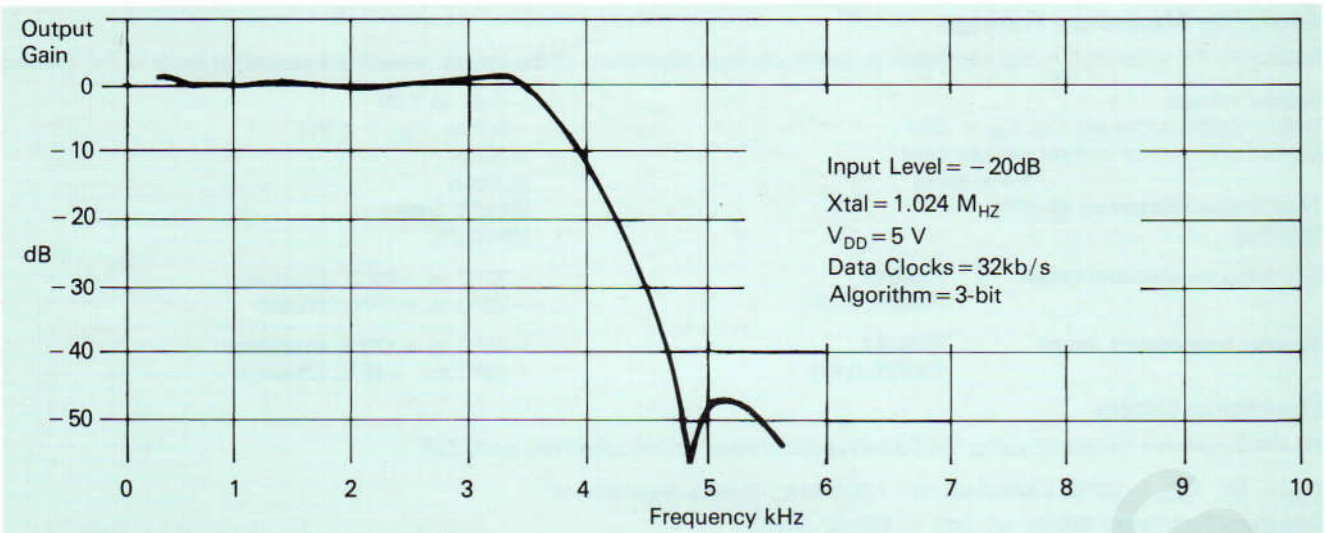


Fig. 5 Typical Codec Frequency Response

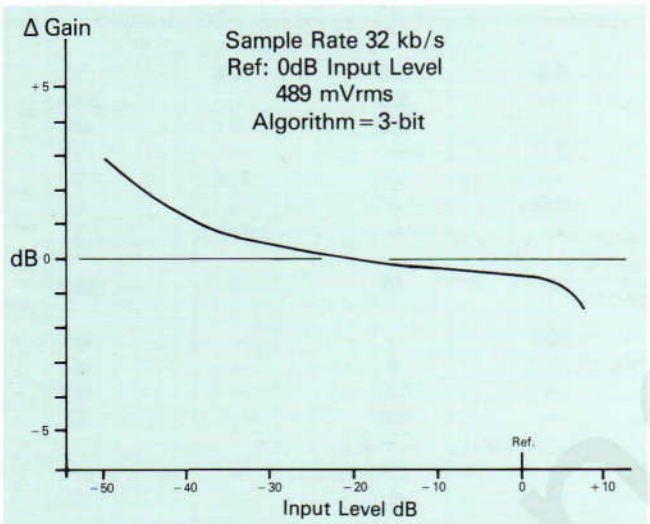


Fig. 6 Typical Variation of Gain with Input Level

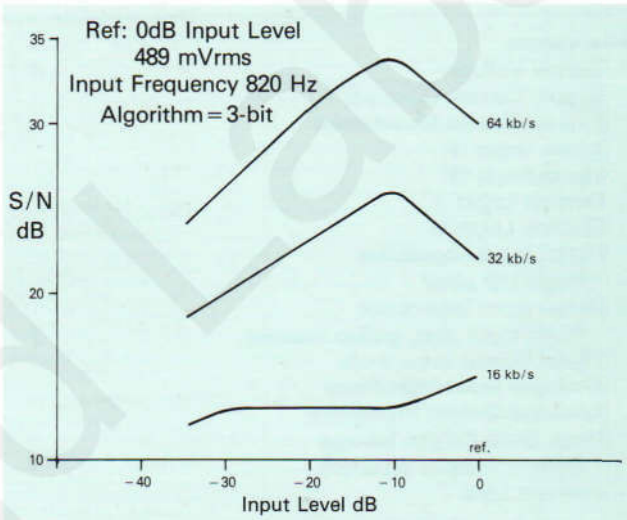


Fig. 7 Typical S/N Ratio with Input Level

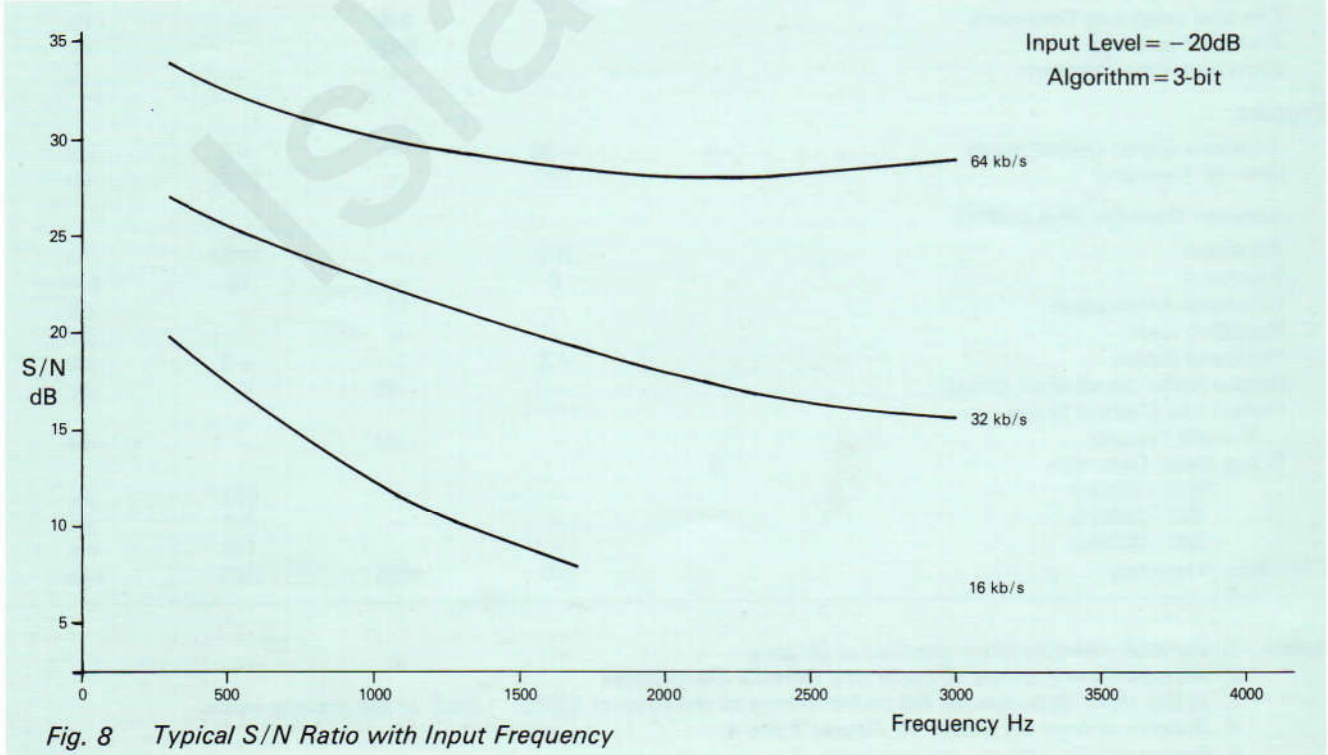


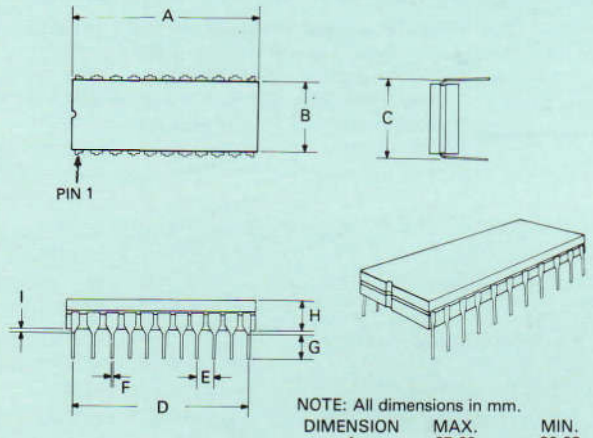
Fig. 8 Typical S/N Ratio with Input Frequency

Package Outlines

The FX609J, the cerdip package, is illustrated in *Figure 9*. The 'LG' version is shown in *Figure 10*, and the 'LH' version in *Figure 11*.

To allow complete identification, the FX609 LG and LH packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4 for LG package, between pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

Fig. 9 **FX609J** *22-pin DIL Package*



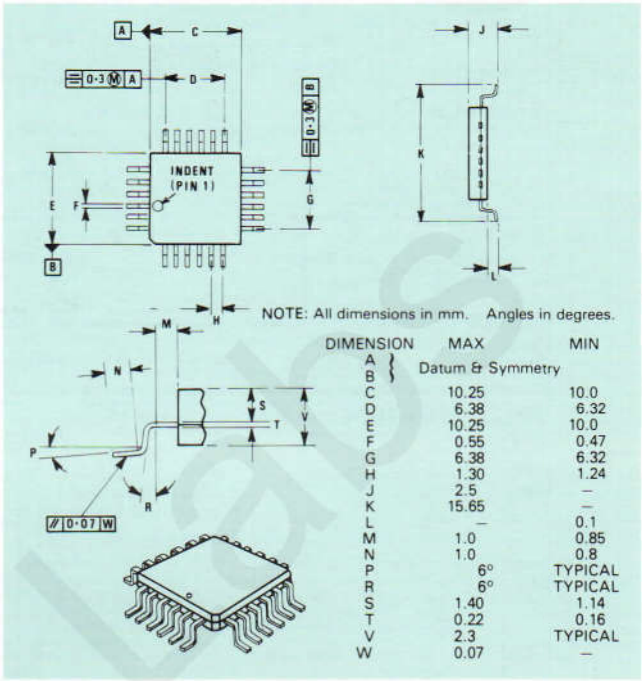
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	27.38	26.98
B	9.75	9.55
C	10.60	10.40
D	25.50	25.30
E	2.54	TYPICAL DIMENSION
F	0.46	
G	4.35	
H	4.27	3.99
I	—	0.5

Handling Precautions

The FX609J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

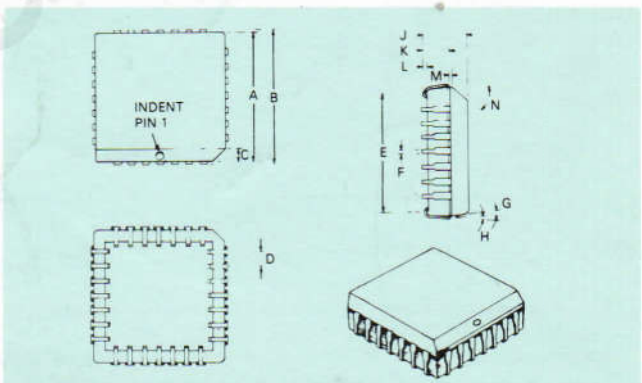
Fig. 10 **FX609LG** *24-pin Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A	Datum & Symmetry	
B		
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	—
K	15.65	—
L	—	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	—

Fig. 11 **FX609LH** *28-lead Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.
A	11.6	11.4
B	12.6	12.3
C	1.1 x 45°	TYPICAL
D	1.3	TYPICAL
E	10.8	10.0
F	0.46	TYPICAL
G	7°	3°
H	7°	3°
J	4.5	4.3
K	2.5	TYPICAL
L	1.1	0.5
M	0.59	TYPICAL
N	45°	TYPICAL

Ordering Information

FX609J — **22-pin cerdip DIL**

FX609LG — **24-pin quad plastic encapsulated, bent and cropped.**

FX609LH — **28-lead Plastic leaded chip carrier.**

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