CML Semiconductor Products

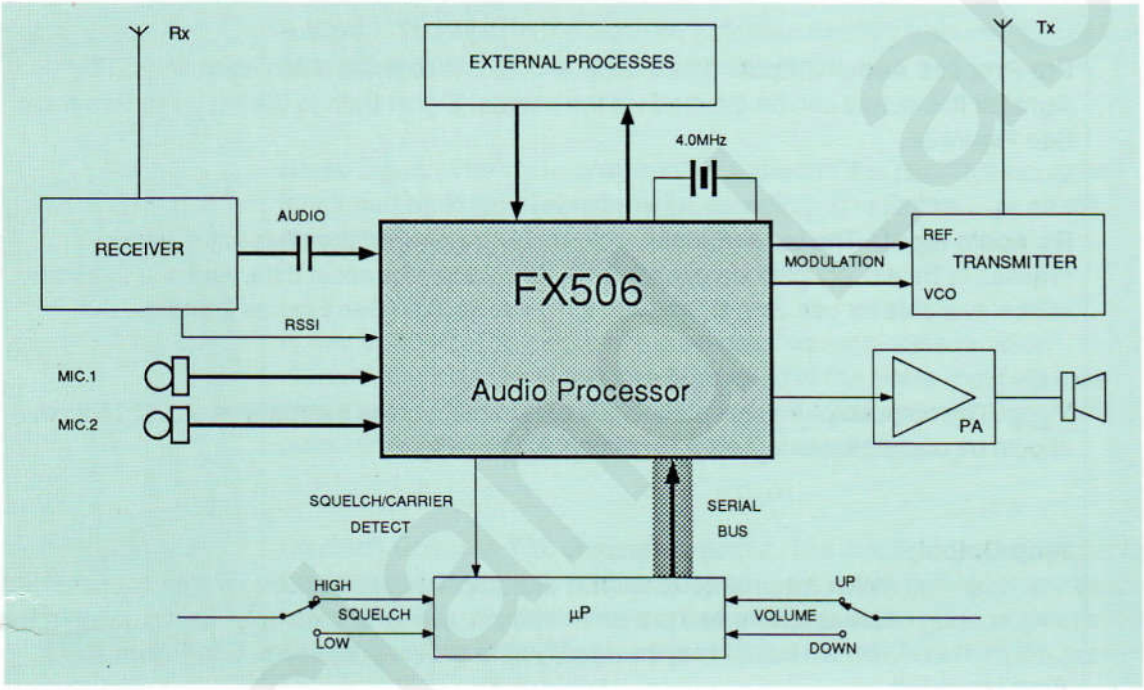
PRODUCT INFORMATION

FX506 Mobile Radio Audio Processor

Publication D/506/1 October 1989
Provisional Issue

Features/Applications

- Full Rx and Tx Filtering to CEPT Standards
- Digital Control of Volume, Noise Squelch and R.S.S.I.
- Tx VOGAD Circuitry
- Serial µP Control of ALL Chip Functions
- Deviation Limiter
- Military/Marine and Mobile Radio Applications
- FM/AM/SSB Applications
- Evaluation Circuit Available
- 16-kbit Data and Voice Scrambler Compatible
- Low-Power 5-Volt CMOS Process



FX506

Brief Description

The FX506 is a µProcessor-controlled, single-chip device containing ALL the circuit elements necessary to perform the audio functions of a mobile (or portable) radio system.

On-chip signal paths include; speech-band/pre- and de-emphasis filters, variable gain/attenuation stages, voice compression and deviation limiter circuitry.

Each function in the signal path can be addressed or by-passed – *providing "real-time," dynamic control* – via an externally produced serial control word. This half-duplex device comprises two serial signal paths.

The Pre-Process path. Intended to set the incoming audio (Rx or Tx) to levels and frequencies suitable for amalgamation with auxiliary systems such as "Frequency Inversion Scrambling," "Sub-Audio" tone or "In-Band" data signalling. This path can be output to external processes or internally routed to the **Post-Process path**.

The Post-Process path can adjust and prepare the input audio (either internal or external) for output to the chosen transmitter driver or loudspeaker amplifier.

Suitably software configured, the FX506, which can operate on Voice, Direct Digital or Tone data, is compatible with FM, AM and SSB type transceivers. Digital gain elements are on-chip for dynamic control and balance of signal levels during manufacturing, test and operation.

System squelch, a separate path, is sourced from either the input signal or Received Signal Strength Indicator (R.S.S.I.) in the radio.

The PC5060, an evaluation printed circuit board, is available to assist in FX506 application design.

The FX506, a low-power 5-volt CMOS device, is available in 24-pin/lead plastic DIL and SMD packages.

Pin Number DIL FX506P	Pin Number Quad FX506LG FX506LS	Function
1		**$\overline{\text{Xtal}}$:** The output of the 4.0MHz on-chip clock oscillator.
2		**Xtal/Clock:** The input to the on-chip 4.0MHz clock oscillator inverter. All oscillator components are included on-chip. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2.
3		**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required.
4		**External Audio Process Input:** The analogue input to the Post-Process path from external audio operations. This input is selected by input serial data and when not selected is connected internally to the Pre-Process Audio Output via the Internal Signal Path. Inputs to this pin should be a.c. coupled via a capacitor, C_7. See Figures 2 and 3.
5		**Pre-Process Audio Output:** The analogue output to external audio operations. The signal at this output can be directed via the Internal Signal Path to the Post-Process path. See Figure 3.
6		**Rx Audio Input:** The input from the radio receiver demodulator. This input, which requires to be a.c. coupled via capacitor, C_6, is selected by serial data. Audio at this input will be available for use as a signal-squelch noise source. See Figures 2 and 3.
7		**V_{BIAS}:** The output of the on-chip analogue bias circuitry, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} via a capacitor, C_1. See Figure 2.
8		**Amp Output:** With external components, this amplifier can be used as a microphone pre-amplifier and pre-emphasis circuit. For a "gain only" configuration a serial resistor may be employed at the Amp Input (-). See Figure 2.
9		**Amp Input (–):**
10		**Mic. Output:** The output of the microphone multiplexer, selected by serial input data. This output should be connected to the Op-Amp Input (-). See Figures 2 and 3.
11		**Mic.1 Input:** These separate microphone audio inputs are individually selected by the serial input data. See Figure 3.
12		**Mic.2 Input:**
13		**V_{SS}:** Negative supply rail (GND).
		Serial data control information is given on Pages 6, 7, 8 and 9 with reference to Figure 3.

Pin Number DIL FX506P	Pin Number Quad FX506LG FX506LS	Function
	14	**Compression Capacitor:** External components connected to this pin provide the required compression time-constant. See Figure 2.
	15	**Audio Output (Rx):** The received audio output from the Post-Process path. This output is data selected and when powersaved is held at V_{BIAS}.
	16	**VCO Ref. Drive Output:** The output to drive the Modulation reference oscillator. This output is data selected and when powersaved is held at V_{BIAS}.
	17	**VCO Drive (Tx) Output:** The output to drive the Modulation VCO. This output is data selected and when powersaved is held at V_{BIAS}.
	18	**R.S.S.I.:** The input to the Squelch Selection circuitry from the radio's Received Signal Strength Indicator output. A data selected input.
	19	**Noise Input:** The noise level can be applied to this pin. This would be the Noise Output integrated by external components, as indicated in Figure 2, or an externally produced noise level.
	20	**Noise Output:** The output of the on-chip "squelch noise rectifier." This output is a half-wave rectified d.c. level that can be applied to the Noise Input via external integrating components. This output could also be used by an external signal detector circuit. This output level is at V_{BIAS} for no input. See Figures 2 and 3.
	21	**Squelch Drive:** A TTL compatible output. The inputs to the comparator are, the logically selected threshold level from the Digital-to-Analogue converter and the selected noise input. This output will be a logic "1" when the selected noise is greater than the set threshold, and a logic "0" when the selected noise is less than the set threshold.
	22	**Serial Clock:** The externally produced serial data loading clock input. See Figure 4. This input has an internal 1MΩ pullup resistor.
	23	**Serial Data:** The controlling, 47-bit serial data input. With $\overline{\text{Chip Select}}$ maintained at a logic "0" the serial data is entered at this pin, loaded bit 46 first, bit 0 last. Detailed information on the allocation and function of serial data bits (0 to 46) is available on Pages 6, 7, 8 and 9. Data load timing should be carried out as described in Figure 4. This input has an internal 1MΩ pullup resistor.
	24	**$\overline{\text{Chip Select}}$:** The data loading control function. During serial loading this input should be operated as shown in Figure 4. New data is latched on the rising edge of this waveform. This input has an internal 1MΩ pullup resistor. Serial data control information is given on Pages 6, 7, 8 and 9 with reference to Figure 3.

External Components and Interfacing

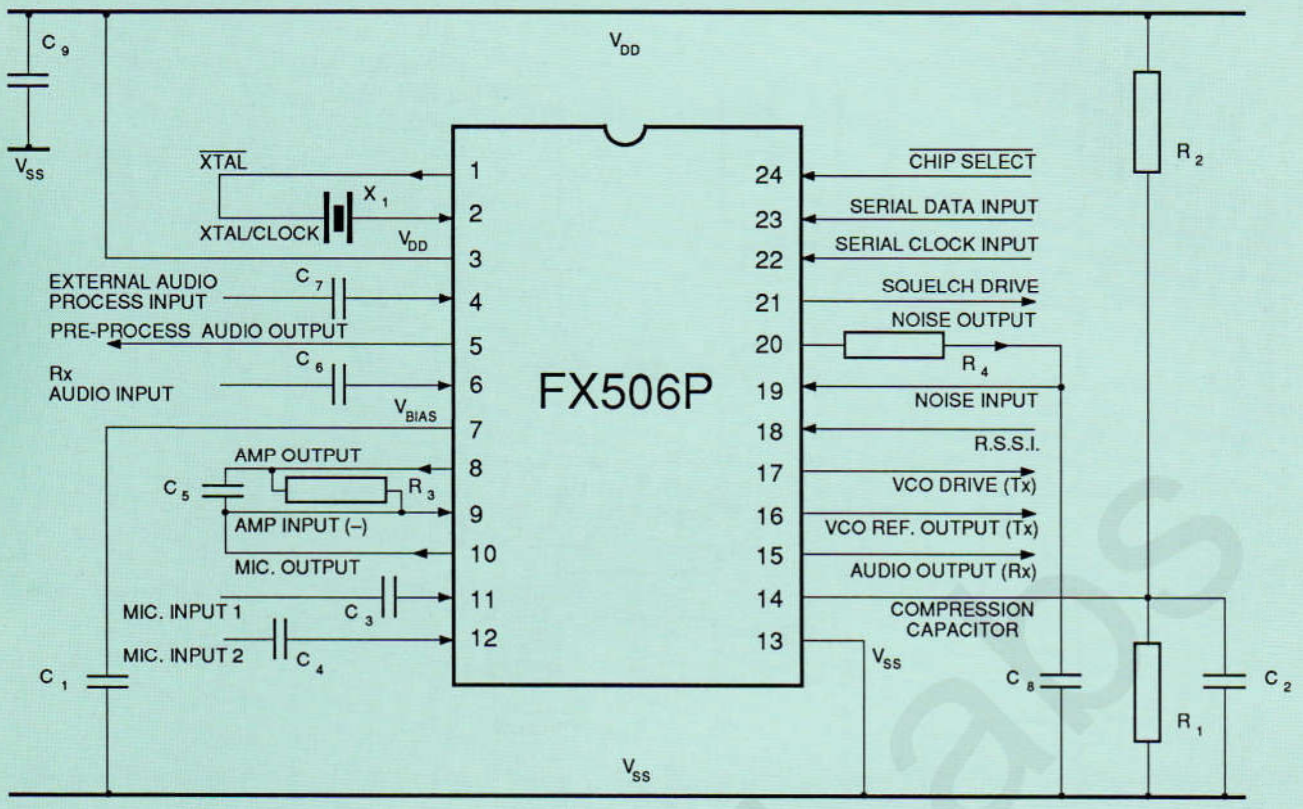


Fig.2 Recommended External Components

Circuit References

Component	Value	Tolerance
R_1	390kΩ	±10%
R_2	100kΩ	±10%
R_3	100kΩ	±10%
R_4	10kΩ	±10%
C_1	1.0µF	±20%
C_2	1.0µF	±20%
C_3	3.3nF	±10%
C_4	3.3nF	±10%
C_5	39pF	±20%
C_6	0.1µF	±20%
C_7	0.1µF	±20%
C_8	0.1µF	±20%
C_9	1.0µF	±20%
X_1	4.0MHz	

Input Components
C_3 or C_4, C_5, R_3. Mic. Input (1 or 2) coupling and Op-Amp gain/pre-emphasis. Component values recommended are to provide gain of 6.0dB at 1kHz. C_3/C_4 or R_3 may be varied to provide alternative gain settings.
For a "gain only" configuration a resistor can be employed at the Amp Input (-).

Compression Time Constant
R_1, R_2, C_2.

Noise "Signal" Integration
R_4, C_8.

Layout Recommendations

Audio microcircuit performance will be affected by external noise.

All external components should be kept as close to the device as possible.

Tracks to the device should be kept short, particularly the Audio and V_{BIAS} inputs.

A "ground-plane" connected to V_{SS} will help to eliminate external pick-up.

Ensure that all inputs (analogue and d.c.) are free from noise.

Xtal/clock and digital tracks should be kept well away from analogue circuitry. Analogue inputs and outputs should be screened wherever possible with high-level outputs isolated from very low-level inputs.

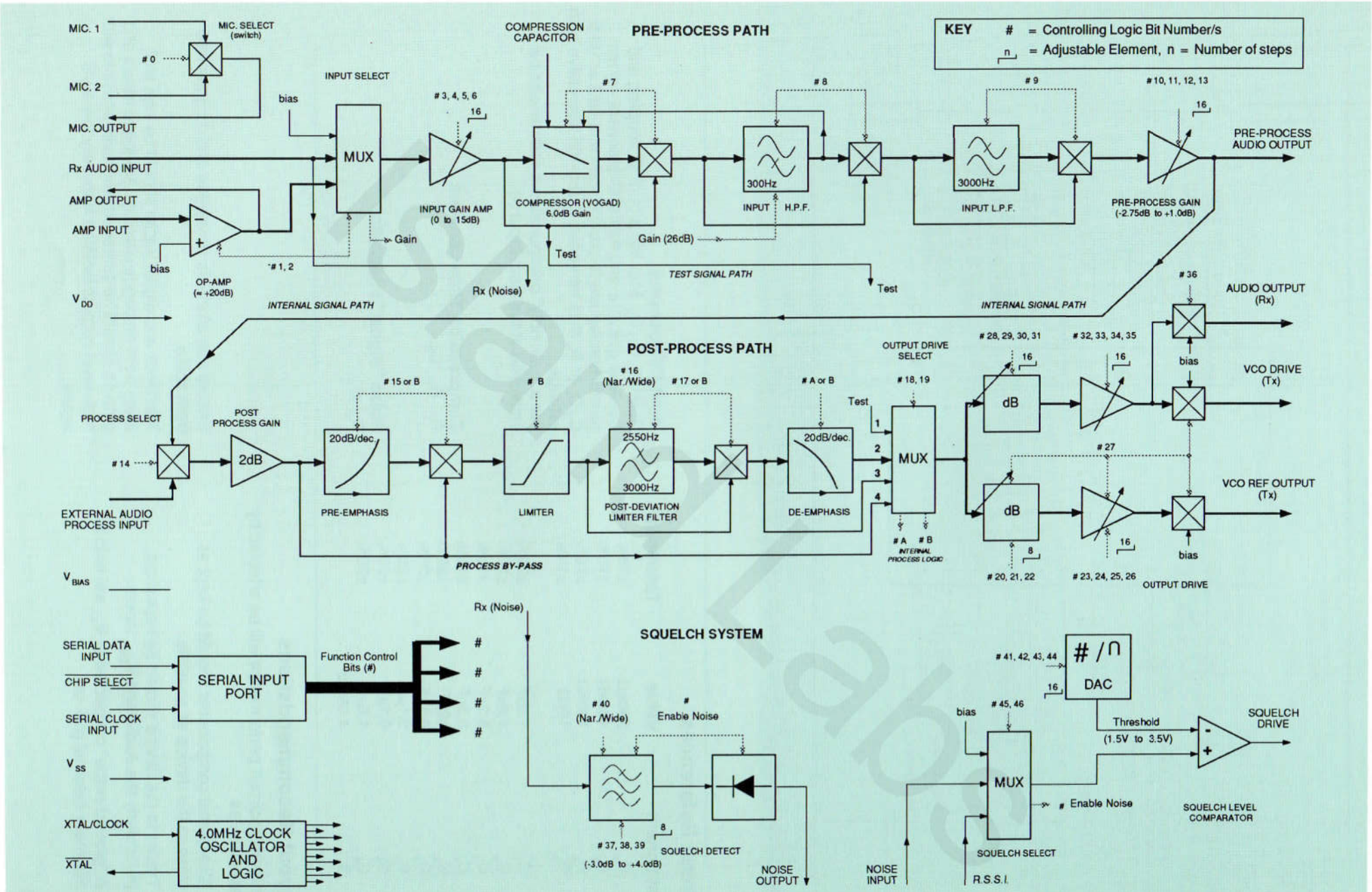


Fig.3 PMR Audio Processor – Facilities

Control bits	Function	Notes
0 0 1	**Mic. Select** – Microphone Input 1 – Microphone Input 2	A multiplexed "microphone" input allowing the use of differing type and level voice inputs.
	Input Op-Amp	With external components, this amplifier can be used as a pre-amplifier and pre-emphasis circuit in the Tx speech path. This gain element is available to adjust the drive level from differing signal sources and microphone sensitivities. Enabled by bits 1 and 2.
1 ***2*** 0 0 1 0 0 1 1 1	**Input Select** – Internal bias path, no input selected. – Selected Microphone Input. Highpass Filter gain set to 26dB. – Rx Audio Input. Powersave Op-Amp. – Internal bias path, no input selected. Powersave Input Op-Amp.	Transmit or receive audio sources are selected, inserting the appropriate path gain for the chosen input. The input path can be set to bias whilst allowing receiver monitoring. Input Op-Amp is enabled for transmit selection.
3 ***4*** ***5*** ***6*** 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**Input Gain Amplifier** – Gain Set 0.0dB 1.0dB 2.0dB 3.0dB 4.0dB 5.0dB 6.0dB 7.0dB 8.0dB 9.0dB 10.0dB 11.0dB 12.0dB 13.0dB 14.0dB 15.0dB	A gain element intended to adjust the drive level to the compressor, catering for differing signal sources and microphone sensitivities.
7 0 1	**Compressor (VOGAD)** – By-pass and powersave compressor. – Enable signal through compressor.	A pre-set, selectable voice amplitude compression circuit, providing optimum drive levels to the transmission medium from differing signal level inputs. The Input Highpass Filter must be used with this element.
8 0 1	**Input Highpass Filter** – By-pass and powersave filter. – Enable Input Highpass Filter.	A 300Hz speech-path shaping lowpass filter. See Figure 5. The filter gain is increased to +26dB when Mic. is selected (bits 1 and 2).
9 0 1	**Input Lowpass Filter** – By-pass and powersave filter. – Enable Input Lowpass Filter.	A 3000Hz speech-path shaping, highpass filter. See Figure 5.
10 ***11*** ***12*** ***13*** 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**Pre-Process Gain** – Gain Set -2.75dB -2.50dB -2.25dB -2.00dB -1.75dB -1.50dB -1.25dB -1.00dB -0.75dB -0.50dB -0.25dB 0dB 0.25dB 0.50dB 0.75dB 1.00dB	An in-line output drive stage providing adjustable gain or attenuation to compensate for level tolerances in the external audio processes and peripherals. The output of this amplifier stage can be routed via an external path, or output to further voice processing (e.g. "Frequency Inversion Voice Scrambling"), or the introduction of Sub-Audio Tones or In-Band data to the system.
		Reference ..... Figure 3

Control bits	Element	Notes
14 0 1	**Process Select** – Pre-Process Internal Path – External Audio Process	To select either the Internal Signal Path or the External Audio Process Input. This external input could be from a "Voice Scrambler" or the composite audio from a Sub-Audio or data signalling system.
	Post-Process Gain	A fixed 2.0dB gain stage.
15 0 1	**Pre-emphasis** – Powersave and by-pass pre-emphasis. – Enable pre-emphasis path.	A selectable pre-emphasis stage set around 1.0kHz, with a characteristic of 6dB per octave. Is also powersaved when Process By-pass is selected (bits 18 and 19).
Internal "B"	**Deviation Limiter**	A selectable, pre-set amplitude limiting stage for deviation control. Powersaved when Process By-pass is selected (bits 18 and 19).
16 0 1	**Post-Deviation Limiter Filter** – Narrow filter bandwidth, cut-off = 2550Hz. – Wide filter bandwidth, cut-off = 3000Hz.	This selectable lowpass filter is adjustable to Narrow (2550Hz) and Wide (3000Hz) bandwidths, allowing for different channel spacing requirements. See Figure 6.
17 0 1	– Powersave and by-pass filter. – Enable filter path.	This filter is also powersaved by internal bit B.
Internal "A or B"	**De-emphasis**	A selectable stage set around 1.0kHz, with a characteristic of 6dB per octave.
18 19 0 0 1 0 0 1 1 1	**Output Drive Selector** – Test Signal Path **1** – Process Path – **2** – Process Path – **3** – Process By-pass Path **4**	To select the path to the Output drive stages. – Via de-emphasis element. – Via de-emphasis by-pass.
20 21 22 0 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 1 1 1	**VCO Reference Drive Attenuator** – Gain Set -28dB -24dB -20dB -16dB -12dB -8.0dB -4.0dB 0.0dB	The in-line control attenuator for the VCO reference channel drive output.
23 24 25 26 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**VCO Reference Drive Amplifier** – Gain Set -2.75dB -2.50dB -2.25dB -2.00dB -1.75dB -1.50dB -1.25dB -1.00dB -0.75dB -0.50dB -0.25dB 0dB 0.25dB 0.50dB 0.75dB 1.00dB	The in-line control amplifier/attenuator for the VCO reference channel drive output.

Reference ..... Figure 3

Control bits	Element	Notes
27 0 1	**Output Control** – Powersave VCO Ref. Amplifier and Attenuator, disable Ref. and Drive Outputs. V_{Bias} at both outputs. – Enable Ref. Tx and VCO Tx Outputs.	
28 29 30 31 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**VCO Drive Attenuator** – Gain Set -48.0dB -44.8dB -41.6dB -38.4dB -35.3dB -32.0dB -28.8dB -25.6dB -22.4dB -19.2dB -16.0dB -12.8dB -9.6dB -6.4dB -3.2dB 0dB	The in-line control attenuator for the VCO Tx channel drive output. This channel is also selected as Audio Output (Rx) under the control of bit 36. This attenuator can be used in a volume control application.
32 33 34 35 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**VCO Drive Amplifier** – Gain Set -2.75dB -2.50dB -2.25dB -2.00dB -1.75dB -1.50dB -1.25dB -1.00dB -0.75dB -0.50dB -0.25dB 0dB 0.25dB 0.50dB 0.75dB 1.00dB	The in-line control amplifier/attenuator for the VCO Tx channel drive output. This channel is also selected as Audio Output (Rx) under the control of bit 36. This amplifier can be used in a volume control application.
36 0 1	**Audio Output (Rx)** – Output at bias, disabled. – Rx Audio Output Enabled.	This function is designated for use in the Rx mode but can be used as a parallel output to the VCO Drive (Tx).
37 38 39 0 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 1 1 1	**Squelch Filter (Gain)** – Gain Set -3.0dB -2.0dB -1.0dB 0dB 1.0dB 2.0dB 3.0dB 4.0dB	The squelch function is set by bits 45 & 46 (Squelch Source Selection). The centre frequency gain of this element is 35dB, data selected gain variations (-3.0dB to 4.0dB) are around this value.
40 0 1	**Squelch Filter** (Narrow/Wide) – Narrow ($fc \approx 18kHz \pm 6.5kHz$). – Wide ($fc \approx 25kHz \pm 8.5kHz$).	For use in wide or narrow channel systems. The squelch function is set by bits 45 & 46 (Squelch Source Selection).

Reference ..... Figure 3

Control bits				Element		Notes
41	*42*	*43*	*44*			
0	0	0	0	**Squelch Threshold Voltage**		The fine squelch adjustment level from the digital-to-analogue converter.
				3.500V d.c.	70.0% V_{DD}	
1	0	0	0	3.366	67.3%	These threshold levels are used as a comparison with the selected input noise voltage (bits 45 and 46).
0	1	0	0	3.233	64.6%	
1	1	0	0	3.100	62.0%	
0	0	1	0	2.966	59.3%	Variation in V_{DD} will produce variation in threshold levels.
1	0	1	0	2.833	56.6%	
0	1	1	0	2.700	54.0%	
1	1	1	0	2.566	51.3%	
0	0	0	1	2.433	48.6%	
1	0	0	1	2.300	46.0%	
0	1	0	1	2.166	43.3%	
1	1	0	1	2.033	40.6%	
0	0	1	1	1.900	38.0%	
1	0	1	1	1.766	35.3%	
0	1	1	1	1.633	32.6%	
1	1	1	1	1.500	30.0%	

45	*46*		
0	0	**Squelch Source Selector**	
1	0	– Internal bias path.	– Enable Detector Filter and Rectifier.
0	1	– Integrated external Noise Input.	– Enable Detector Filter and Rectifier.
1	1	– R.S.S.I. Input.	– Enable Detector Filter and Rectifier.
		–	– *(Do not use this setting, reserved for future designs)*

Internal "A"
Selects the De-emphasis element in the Process path, powersaves the De-emphasis element in Process or De-emphasis By-pass (bits 18 and 19).

Internal "B"
Powersaves the Post-Process path when Process By-pass selected (bits 18 and 19).

Rx Noise Path
Any audio present at the Rx Audio Input will also be available via the squelch filter (when enabled) for use as a squelch detection level. This means that the FX506 can be set to "idle" with the majority of circuit elements powersaved until a "significant noise" level is used to produce a "squelch drive output."

Test Signal Path
This path, when selected, can be used as a direct path, via the Output Drive Selector (bits 18 and 19), to dynamically set and balance the VCO drive and reference output levels.

Powersave
The list below briefly shows the elements that can be powersaved via serial control:

Pre-Process Path: Op-Amp – Compressor circuit – Input Highpass Filter – Input Lowpass Filter.

Post-Process Path: Pre-emphasis – Limiter – Post Deviation Limiter Filter – De-emphasis – VCO Ref. Attenuator and Amplifier.

Squelch System: Bandpass Filter – Squelch Rectifier.

The following elements are active at all times:

Input Gain Amp – Pre-Process Gain Amp – Post-Process Amp (+2.0dB) – VCO Drive Attenuator and Amplifier – Digital-to-Analogue Converter – Squelch Level Comparator.

Reference ..... Figure 3

Serial Control Bits – Loading and Timing Information

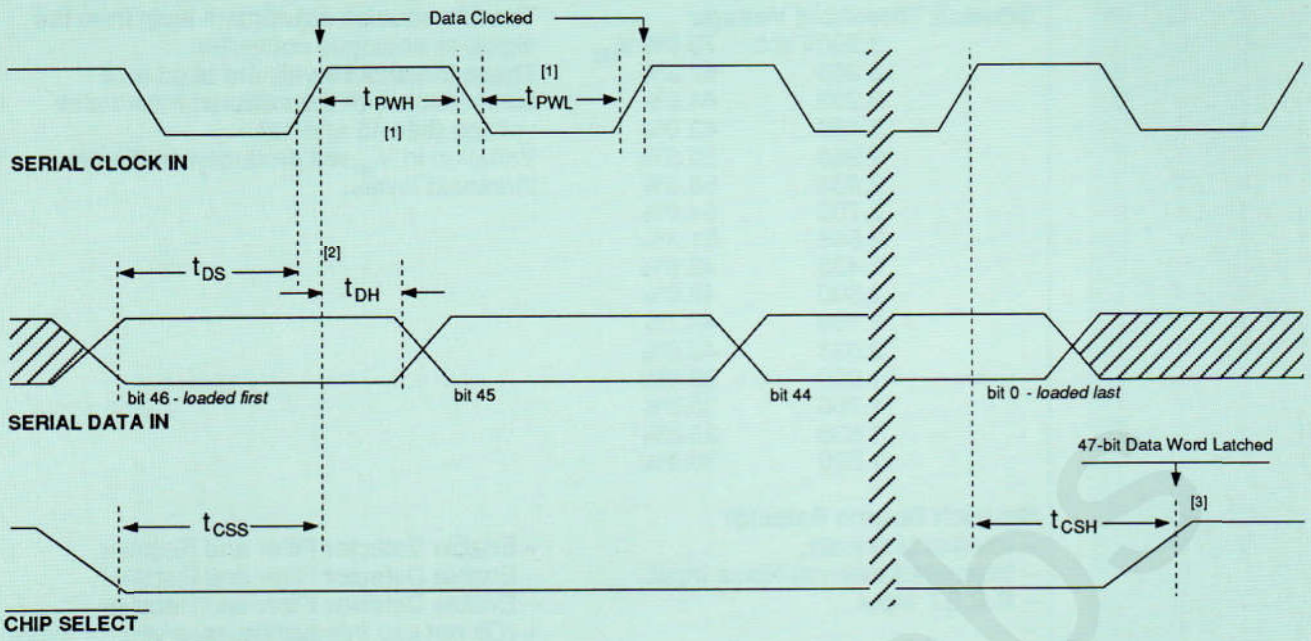


Fig.4 Data Load Timing

Data Loading

Serial Data bits, whose functions are described on Pages 6, 7, 8 and 9, are loaded to the FX506 using the timing format illustrated on this page. All 47 bits must be loaded. Data is loaded bit 46 first, bit 0 last.

Function			Min.	Typ.	Max.	Unit
Serial Clock	[1]					
'High' Pulse Width		t_{PWH}	600	–	–	ns
'Low' Pulse Width		t_{PWL}	600	–	–	ns
Serial Data	[2]					
Data Set-Up Time		t_{DS}	360	–	–	ns
Data Hold Time		t_{DH}	120	–	–	ns
Chip Select	[3]					
Select Set-Up Time		t_{CSS}	600	–	–	ns
Select Hold Time		t_{CSH}	600	–	–	ns

[1] The Serial Clock pulses do not have to be symmetrical, as shown above, but pulse lengths must conform to the "minimum" time specification.

[2] Individual data bits (logic "1" or "0") are loaded to the device on the rising edge of the Input Serial Data clock pulse, the data hold period (t_{DH}) is to ensure that the data level is steady when it is sampled.

[3] The full 47-bit data word is latched into the device on the rising edge of the Chip Select waveform, at this time the loaded data is acted upon and the circuit configuration will change.

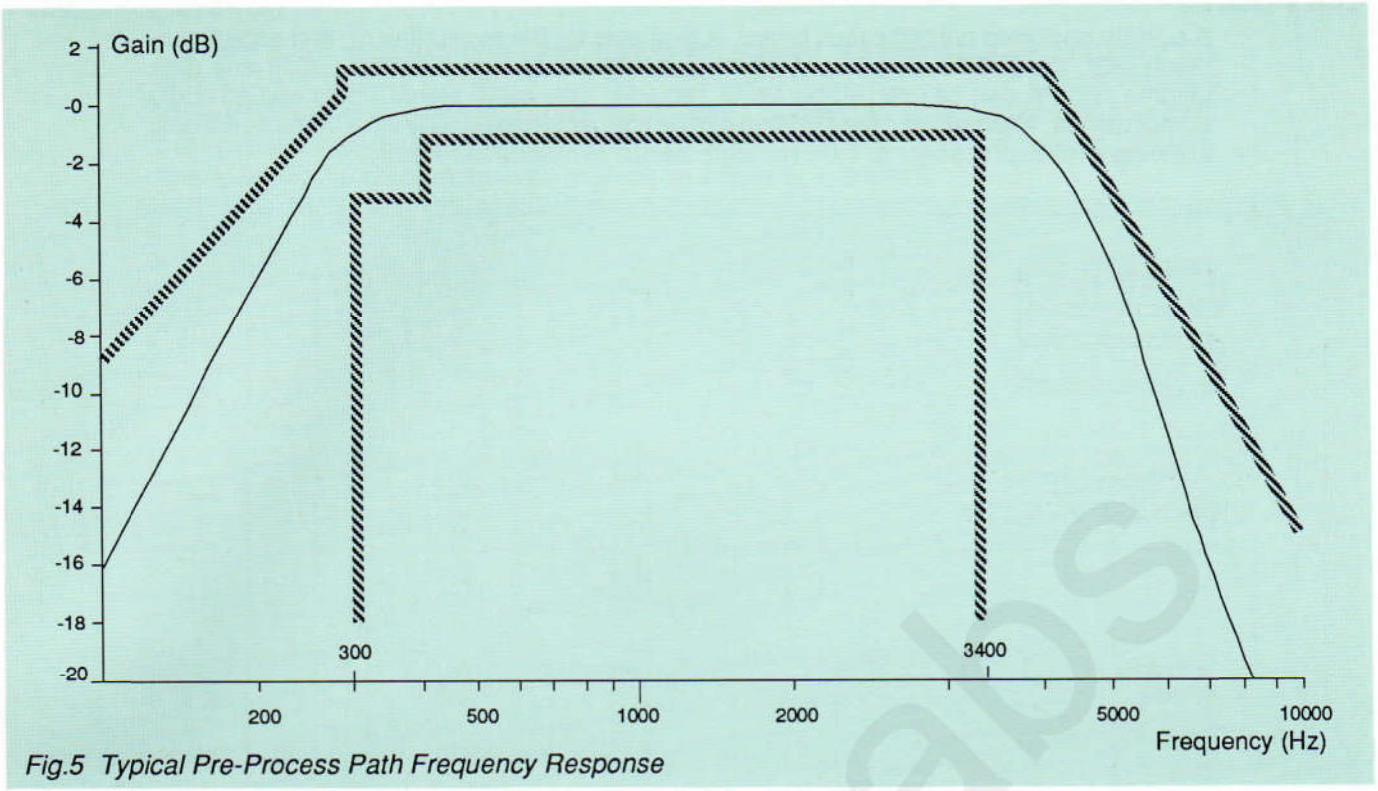


Fig.5 Typical Pre-Process Path Frequency Response

System Frequency Characteristics

Figure 5 shows a typical, response curve of the Pre-Process path, in receive mode, set against the device specification. The general characteristic shape is produced by the Input Highpass and Lowpass Filters, without the pre-emphasis element.

Figure 6 shows a typical response curve of the Post-Process path set against the device specification. The general characteristic shape is produced by the Post-Deviation Limiter Filter, without the de-emphasis element.

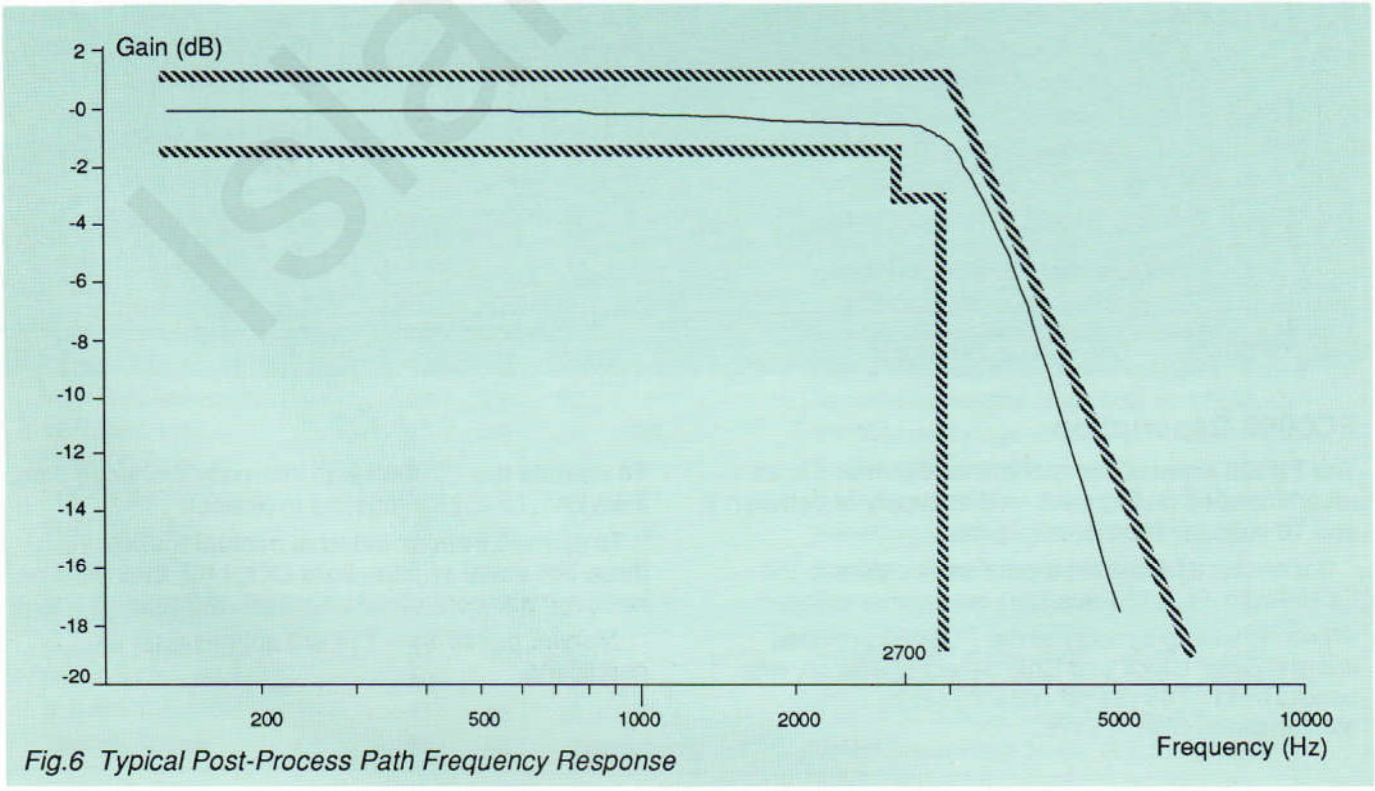


Fig.6 Typical Post-Process Path Frequency Response

Application Information

The PC5060

A custom designed printed circuit board, is available for the evaluation of, and experimentation with, the FX506. The board, which consists serial data switches, clock and data loading system, can be used stand-alone, requiring only audio signal inputs and an audio output device. Alternatively, the PC5060 can be connected externally via a 3-line serial bus, allowing a microprocessor or external logic device to control the FX506.

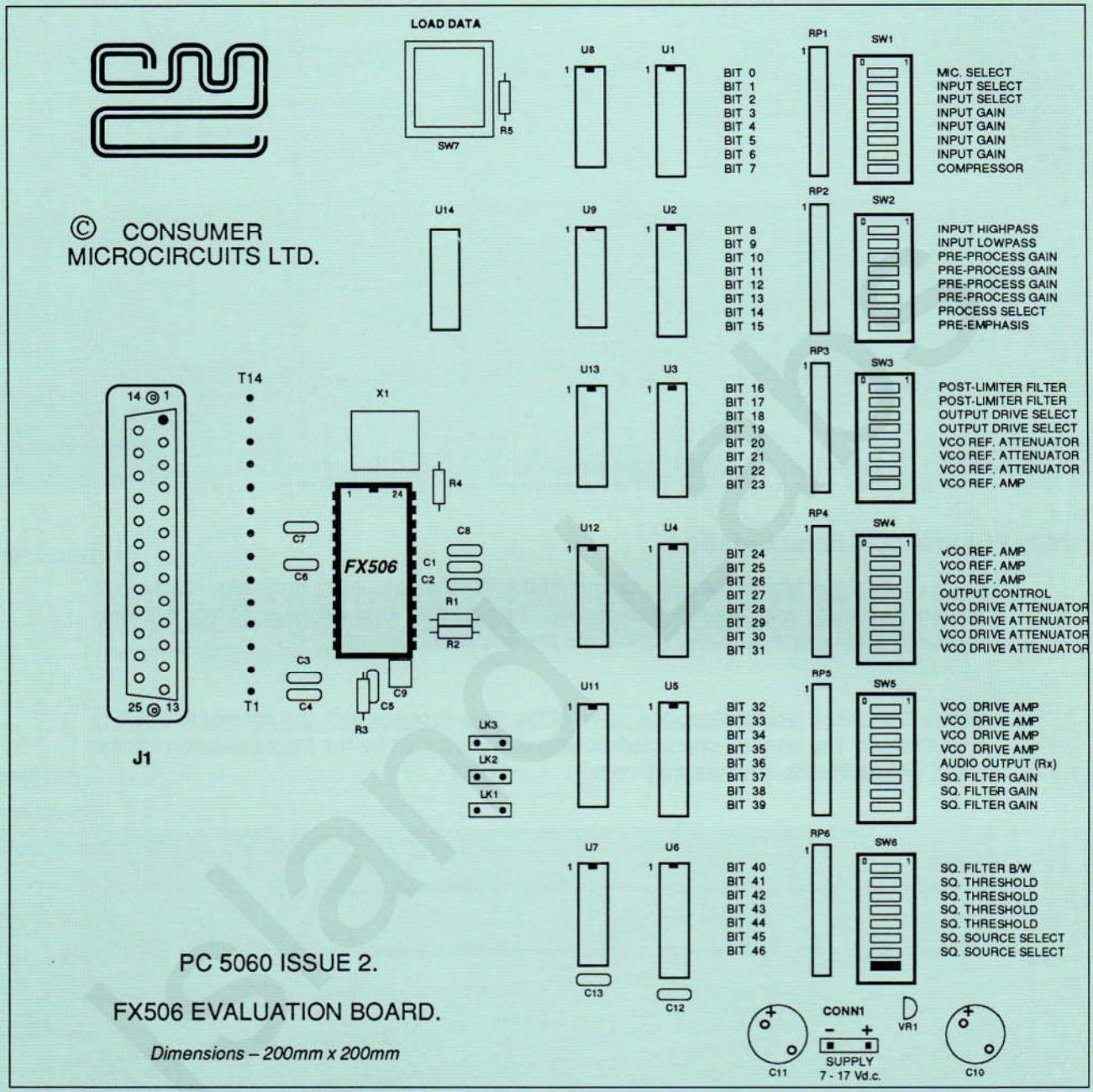


Fig.7 PC5060 – The Evaluation Board

PC5060 Description

The FX506 external component configuration is as recommended on Figure 2. A d.c. supply of between 7 and 16 volts, at 100mA, is required.

Connector J1 provides inputs and outputs to the FX506 with T1 – T14 available as monitor points.

The remaining circuitry of the PC5060 provides internal Data, Clock and Chip Select operation, with control bits 0 – 46 (Serial Data In) set by switch combinations SW1 – SW6.

To operate the PC5060 with internally produced data, links LK1, LK2, LK3 must be in position.

To operate from an external microprocessor via a three-line serial system, links LK1, LK2, LK3 must be removed and control data applied via J1 pins 1 – 3.

Monitor points T1 – T14 are active under all conditions.

Application Information .....

PC5060 Operation

Connect audio and data inputs and outputs as required, via connector J1. Provide a d.c. supply (7 – 16 volts @ 100mA) to CONN1, observing correct polarity. Interface connections to the PC5060 via connector J1 are given in Table 1. Suggested examples of circuit element configurations are given on Pages 14 and 15. A full 47-bit word must be entered for every operation. Serial data information is given on Pages 6, 7, 8 and 9.

J1 Pin	Monitor	Function	J1 Pin	Monitor	Function
	T14	Mic. Out	7	T7	Rx Audio In
1	T13	**Chip Select (LK2)**	8	T6	R.S.S.I.
2	T12	**Serial Data In (LK1)**	9	T5	VCO Drive (Tx)
3	T11	**Serial Clock In (LK3)**	10	T4	VCO Ref. (Tx)
4	T10	Squelch Drive	11	T3	Audio Out (Rx)
5	T9	Ext. Audio Process In	12	T2	Mic. 1 In
6	T8	Ext. Audio Process Out	13	T1	Mic. 2 In

Table 1 PC5060 Interface Connections

Internal Data Control

Ensure links LK1, LK2, LK3 are in position.
Links select the source of the Chip Select, Serial Data and Serial Clock inputs.

Apply a suitable audio signal level. Audio specifications are detailed on the "Specification" page.

Using switches SW1 – SW6 set the required serial control data word for the FX506 functions (bits 0 – 46).

Load the set data by momentarily pushing SW7 "Load Data." Do not operate the PC5060 from external sources with the links in position.

External Data Control

Remove links LK1, LK2, LK3 from the board.

Apply a suitable audio signal level. Audio specifications are detailed on the "Specification" page.

Ensure that Chip Select, Serial Data and Serial Clock logic lines are connected to the PC5060 via J1.

Load and latch the required serial control data word for the FX506 functions (bits 0 – 46) from the microprocessor, as described in the Timing Diagram Figure 4.

Pre-Process Path	**Bit**				
Mic. Select	0	*(loaded last)*			Choice of two microphone (Tx) inputs.
Input Select	1	2			Transmit, Receive and Gain Amp inputs.
Input Gain	3	4	5	6	Variable gain stage 0dB to 15dB.
Compressor	7				Enable or by-pass Compressor.
Input Highpass	8				300Hz Lowpass filter stage.
Input Lowpass	9				3000Hz Highpass filter stage.
Pre-Process Gain	10	11	12	13	Variable gain stage -2.75dB to 1.0dB.
Post-Process Path	**Bit**				
Process Select	14				Select Internal or External signal path.
Pre-Emphasis	15				Enable or by-pass Pre-Emphasis.
Post-Limiter Filter	16	17			Enable or by-pass and select bandwidth of filter.
Output Drive Select	18	19			Select Process, By-pass or Test paths.
VCO Ref. Attenuator	20	21	22		Variable attenuation stage 0dB to -28dB.
VCO Ref. Amp	23	24	25	26	Variable gain stage -2.75dB to 1.0dB.
Output Control	27				Enable or powersave output drives.
VCO Drive Attenuator	28	29	30	31	Variable attenuation stage 0dB to -48dB.
VCO Drive Amp	32	33	34	35	Variable gain stage -2.75dB to 1.0dB.
Audio Out (Rx)	36				Enable or bias Audio Output (Rx).
Squelch System	**Bit**				
Squelch Filter Gain	37	38	39		Variable gain stage, 35dB, -3.0dB /+4.0dB .
Squelch Filter B/W	40				Select filter frequency Narrow/Wide (18/25kHz).
Squelch Threshold	41	42	43	44	Threshold voltage range 1.5v to 3.5v.
Squelch Source	45	46	*(loaded first)*		Select Source from Noise, R.S.S.I. or bias.

Suggested Evaluation Tests and Settings

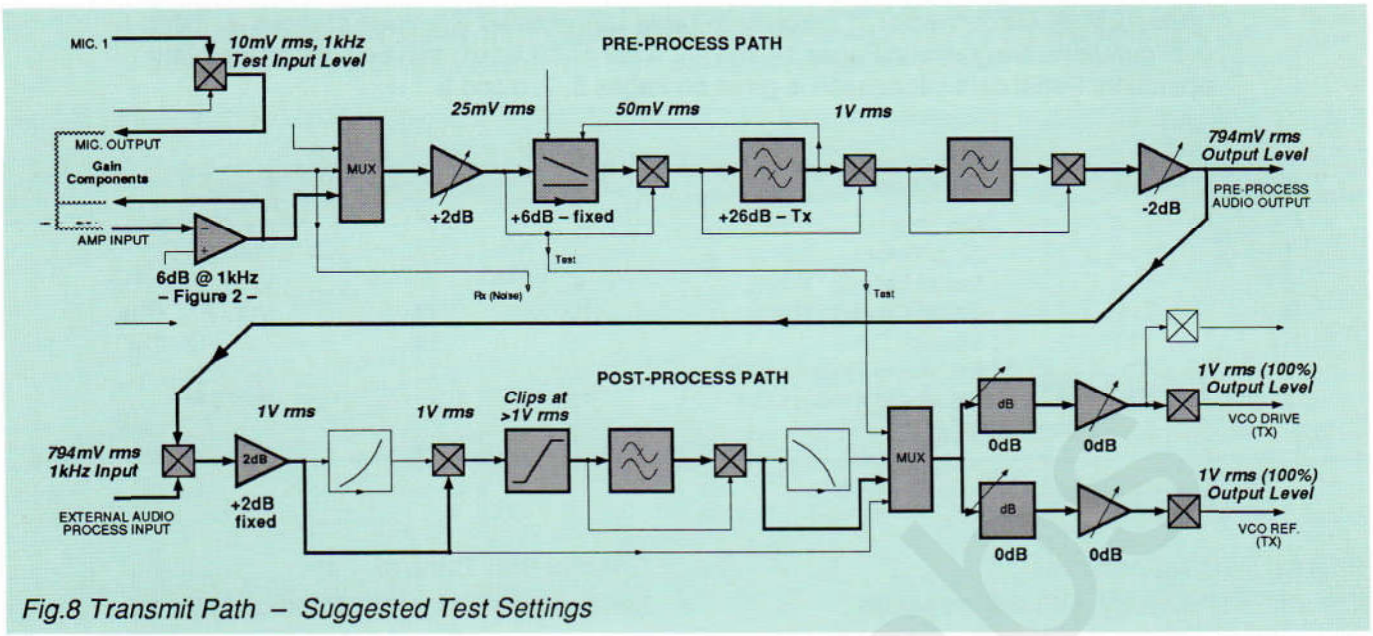


Fig.8 Transmit Path – Suggested Test Settings

Active elements used in the signal path.

Powersaved or by-passed elements that are not employed in the signal path.

Active elements used in the squelch path.

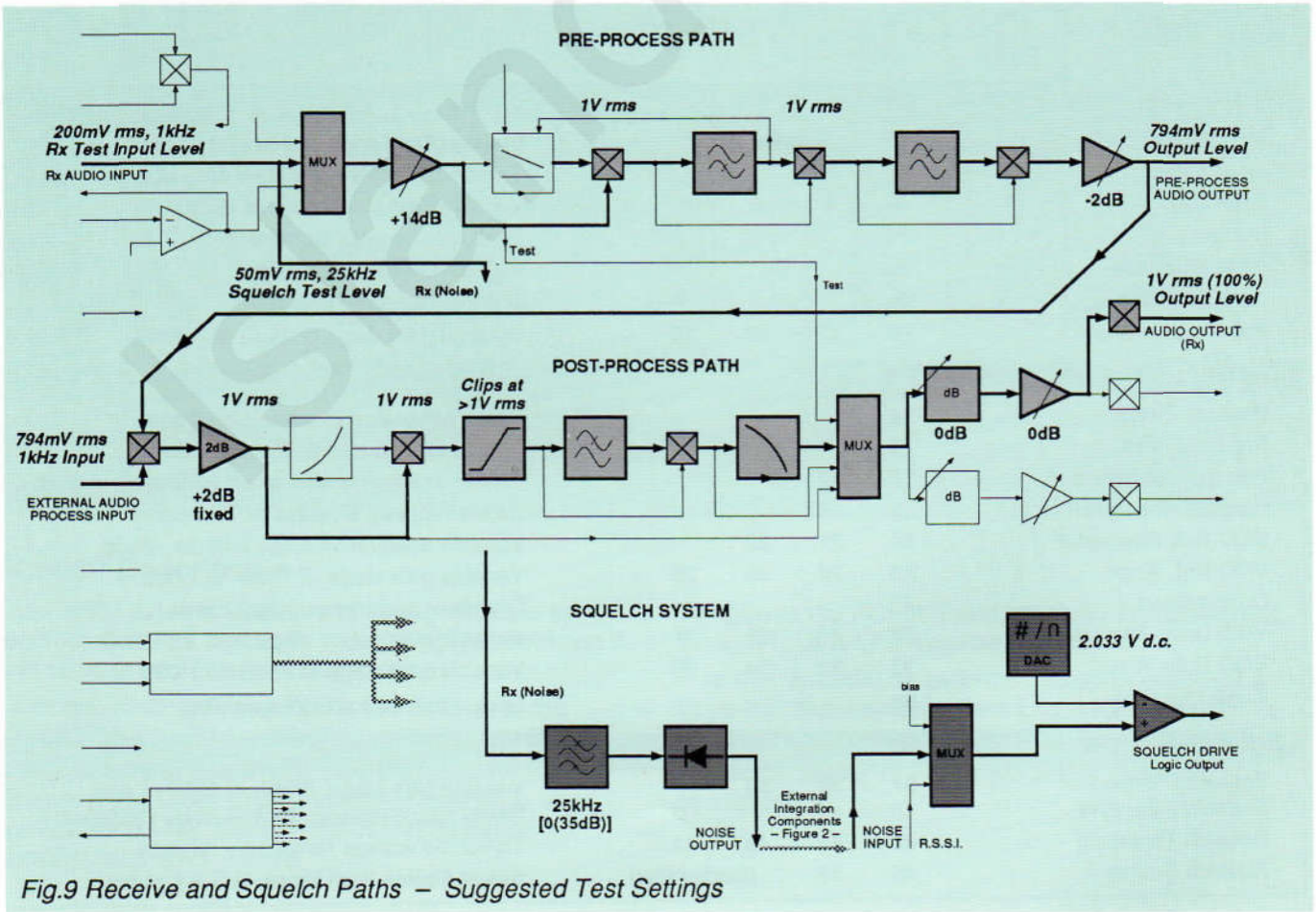


Fig.9 Receive and Squelch Paths – Suggested Test Settings

Suggested Evaluation Tests and Settings

Operational Information

The functions of the FX506 are selected and controlled using the 47-bit Serial Data Input. This application section (pages 12, 13, 14 and 15) assists in the familiarization of control by providing example operational paths and system confidence tests.

The signal levels employed in these examples are to demonstrate the functions of the device. Maximum and minimum operational signal levels are detailed in the "Specification" pages. A final output signal level of 1.0 volt rms is considered, operationally, to be 100% (FM deviation).

Set-up and enter the example data word in accordance with Figures 2 and 4, or using the PC5060 Evaluation System. Test the FX506 using levels and points detailed in Tables 2, 3 and 4.

Experimentation will indicate the signal element configuration and required control settings for various input and output levels.

Control Information is available on Pages 6, 7, 8 and 9

Transmit Path – *The Serial Data word below will produce the transmit element configuration shown in Figure 8.*

bit 0 – **01001001 111100X0 X1011111 10111111 11010XXX XXXXX00** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 1kHz)	Output	Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Mic. 1	10	Pre-Process Audio	794	Bit 14 = X	
2	Ext. Audio Process In	794	VCO Drive and Ref.	1000	Bit 14 = "1"	100%
3	Mic. 1	6	Pre-Process Audio	467	Bit 14 = X	60%
4	Ext. Audio Process In	467	VCO Drive and Ref.	600	Bit 14 = "1"	60%
5	Mic. 1	6	VCO Drive and Ref.	600	Bit 14 = "0"	60%
6	Mic. 1	60	VCO Drive and Ref.	1000	Bit 14 = "0" Comp. & Limit test	100%

Table 2 Transmit Path Operational Check

Receive Path – *The Serial Data word below will produce the receive element configuration shown in Figure 9.*

bit 0 – **X0101110 111100X0 X110XXXX XXX01111 11011XXX XXXXX00** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 1kHz)	Output	Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Rx Audio In	200	Pre-Process Audio	794	Bit 14 = X	
2	Ext. Audio Process In	794	Audio Out (Rx)	1000	Bit 14 = "1"	100%
3	Rx Audio In	123	Audio Out (Rx)	600	Bit 14 = "0"	60%
4	Rx Audio In	123	Audio Out (Rx)	600±	Bit 14 = "0" vary bits 28 – 35 for Volume	60%±

Table 3 Receive Path Operational Check

Squelch Path – *The Serial Data word below will produce the squelch element configuration shown in Figure 9.*

bit 0 – **X00XXXX0 00XXXXX0 X0XXXXXX XXX0XXXX XXXX0110 1110110** – bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 25kHz)	Output	Level	Note
1	Rx Audio In	0	Squelch Drive	logic "1"	No noise – "Noise Out" = V_{BIAS}
2	Rx Audio In	50.0	Squelch Drive	logic "0"	Noise In – "Noise Out" decreases

Table 4 Squelch Path Operational Check

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX506P**	-30°C to +70°C (plastic)
	FX506LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	**FX506P**	-40°C to +85°C (plastic)
	FX506LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Audio level 0dB ref: = 600mV rms *(60% deviation, FM).*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All Elements Enabled)		–	8.0	–	mA
(Maximum Powersave)		–	3.0	–	mA
Dynamic Values					
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Input Impedances					
Digital		0.1	1.0	–	MΩ
Mic.1 or 2		–	1.0	–	kΩ
Rx Audio		50.0	–	–	kΩ
External Audio Process		1.0	–	–	MΩ
Amp Input		1.0	–	–	MΩ
Noise, R.S.S.I.		1.0	–	–	MΩ
Output Impedances					
Pre-Process Audio		–	–	3.0	kΩ
Audio Out (Rx)		–	–	3.0	kΩ
VCO Drive and Ref. Out		–	–	3.0	kΩ
Squelch Drive (Logic "1")		–	1.25	–	kΩ
(Logic "0")		–	150	–	Ω
Noise Output (Diode conducting)		–	10.0	–	kΩ
(Diode not conducting)		–	400	–	kΩ
Signal Path Switch Isolation (Disabled)					
Switches		40.0	–	–	dB
Test Path		–	80.0	–	dB
Signal Input Levels	11				
Mic.1 or 2		1.0	–	100	mV rms
Rx Audio		–	123	200	mV rms
External Audio Process		–	–	795.0	mV rms
Noise, R.S.S.I.	2	–	–	5.0	V
Signal Output Levels	11				
Pre-Process Audio		–	600	1000	mV rms
VCO – (Drive, Ref.)		–	–	1000	mV rms
Audio (Rx)		–	–	1000	mV rms
Variable Element Step Tolerance					
Input Gain Amp		–	–	± 30.0	%
Pre-Process Gain		–	–	± 40.0	%
VCO Ref. Attenuator		–	–	± 12.5	%
VCO Drive Attenuator		–	–	± 15.625	%
VCO Amplifiers (Drive and Ref.)		–	–	± 40.0	%

Specification .....

Characteristics		See Note	Min.	Typ.	Max.	Unit
Output Distortion						
Output Signal-to-Noise Ratio		3	–	45.0	48.0	dB
Total Harmonic Distortion Level		3	–	–	-40.0	dB
Compressor						
Dynamic Range			–	30.0	–	dB
Attack Time			–	0.55	–	ms
Decay Time			–	8.5	–	ms
Deviation Limiter						
Input Thresholds		4	–	2.828	–	V p–p
Frequency Responses						
Pre-Process Path – *Figure 5*		6				
Passband Frequencies (-3dB)			300	–	3400	Hz
Passband Ripple	(300Hz - 400Hz)	5	-3.0	–	1.0	dB
	(400Hz - 3400Hz)	5	-1.5	–	1.0	dB
Stopband Attenuation	(f = 5kHz)		3.0	4.2	–	dB
High Frequency Roll-off	(f = >5kHz, <20kHz)		12.0	–	–	dB/oct.
Stopband Attenuation	(f = 250Hz)		–	2.3	–	dB
Low Frequency Roll-off	(f = <250Hz)		6.0	–	–	dB/oct.
Post-Process Path – *Figure 6*		7				
Wideband : Lowpass Frequency (-3dB)			–	–	3000	Hz
Passband Ripple	(< 2700Hz)	8	-1.5	–	1.0	dB
	(2700Hz - 3000Hz)	8	-3.0	–	1.0	dB
Stopband Attenuation	(f = 5kHz)		12.2	17.0	–	dB
High Frequency Roll-off	(f = >3kHz,<20kHz)		18.0	–	–	dB/oct.
Narrowband: Lowpass Frequency (-3dB)			–	–	2550	Hz
Passband Ripple	(< 2300Hz)		-1.5	–	1.0	dB
	(2300Hz - 2550Hz)		-3.0	–	1.0	dB
Stopband Attenuation	(f = 4.25kHz)		12.2	17.0	–	dB
High Frequency Roll-off	(f = >2.3kHz,<5.1kHz)		18.0	–	–	dB/oct.
Pre-emphasis: Passband Frequencies			300		3000	Hz
	Gain at 1kHz		–	0	–	dB
	Slope Characteristic	9	–	6.0	–	dB/oct.
De-emphasis: Passband Frequencies			300		3000	Hz
	Gain at 1kHz		–	0	–	dB
	Slope Characteristic	9	–	6.0	–	dB/oct.
Squelch Bandpass Filter						
Centre Frequency Gain	(Wide and Narrow)		–	35.0	–	dB
Selectable Gain	(8 x 1.0dB steps)	10	-3.0	–	4.0	dB
Narrow Band:						
Centre Frequency	(fc)		–	18.75	–	kHz
Bandwidth	($fc \pm$)		–	6.5	–	kHz
Wideband:						
Centre Frequency	(fc)		–	25.5	–	kHz
Bandwidth	($fc \pm$)		–	8.5	–	kHz

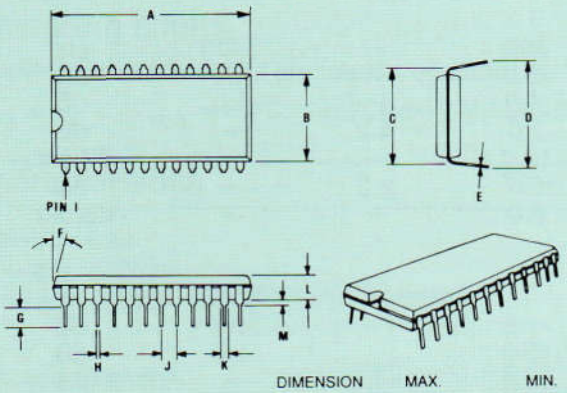
Notes

1. A percentage of the applied V_{DD} (70% or 30%).
2. These inputs are compared internally with the Digital-to-Analogue converter.
3. With a signal output level of 600mV rms, measured in a 30.0kHz bandwidth.
4. Levels at the input of the Limiter element, centred about V_{BIAS} (note 2).
5. This parameter remains within specification when pre-emphasis is employed.
6. With both Input H.P.F. and L.P.F. in circuit, but without pre-emphasis.
7. With Limiter B.P.F., but without de-emphasis characteristics.
8. This parameter remains within specification when de-emphasis is employed.
9. Accuracy = ± 0.5dB from nominal slope characteristic.
10. The gain variation around the centre frequency (fc).
11. See Page 15 (Suggested Evaluation Tests) for information on gain element settings.

Package Outline

The FX506P, the dual-in-line package is shown in Figure 10. The 'LG' version is shown in Figure 11 and the 'LS' version in Figure 12. To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

*Fig.10 **FX506P** 24-pin DIL Package*



Note: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	31.85	31.65
B	13.82	13.61
C	15.75	15.11
D	17.02	15.75
E	0.254	TYPICAL
F	7°	TYPICAL
G	3.43	2.92
H	0.46	
J	2.54	TYPICAL
K	1.52	
L	3.91	3.71
M	0.75	TYPICAL

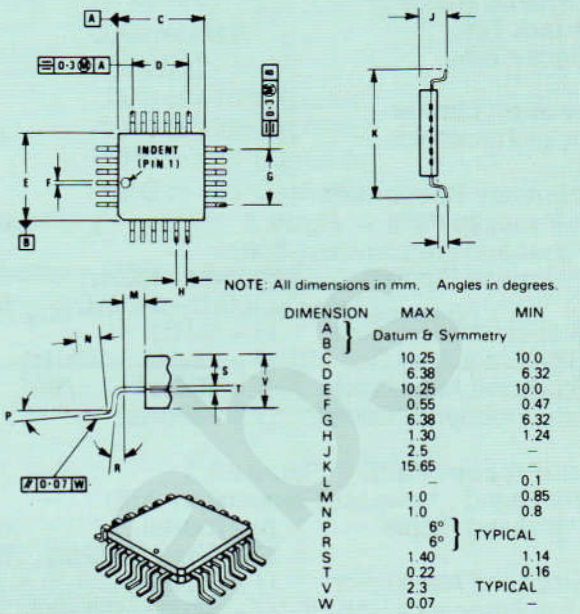
Ordering Information

FX506P	24-pin plastic DIL
FX506LG	24-pin quad plastic encapsulated bent and cropped
FX506LS	24-lead plastic leaded chip carrier
PC5060	FX506 Evaluation Printed Circuit Board – (compatible with a 24-pin DIL device)

Handling Precautions

The FX506 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

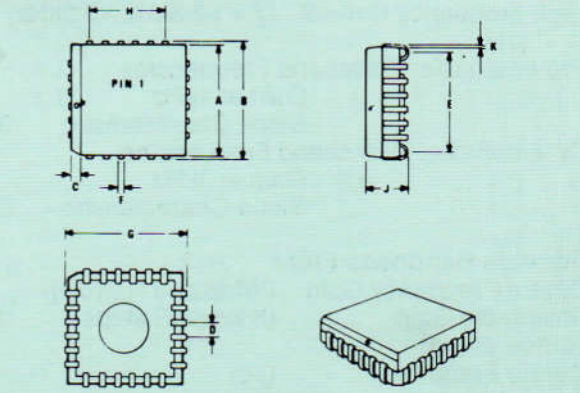
*Fig.11 **FX506LG** 24-pin Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	–
K	15.65	–
L	–	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	–

*Fig.12 **FX506LS** 24-lead Package*



NOTE: All dimensions in mm.

DIMENSION	MAX.		MIN.
A	10.25		10.00
B	11.0		10.20
C		1.14 x 45° typical	
D		1.27 typical	
E	9.65		8.64
F	0.55		0.47
G	11.0		10.20
H		6.35 typical	
J	3.50		3.25
K	0.22		0.16

CONSUMER MICROCIRCUITS LIMITED
1 WHEATON ROAD
WITHAM - ESSEX CM8 3TD - ENGLAND

Telephone: (0376) 513833
Telex: 99382 CMICRO G
Telefax (0376) 518247