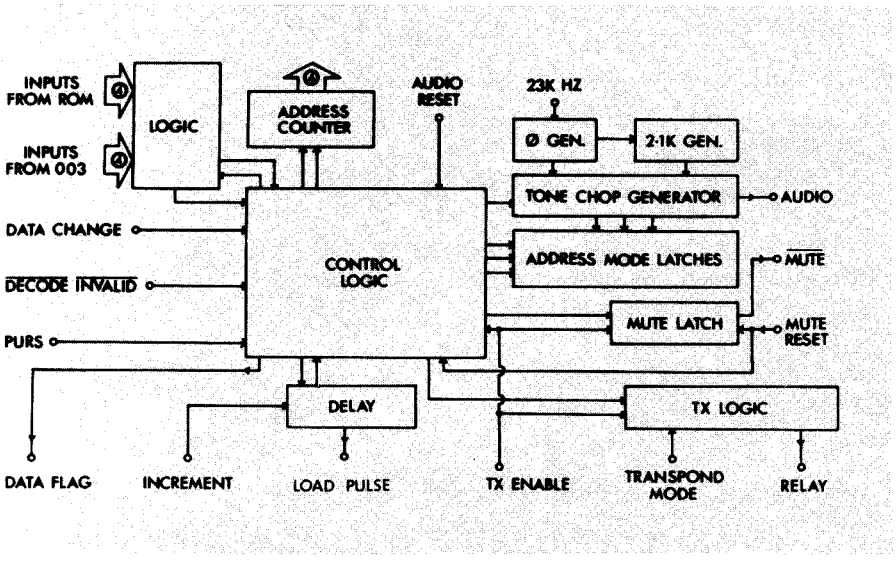
CONSUMER MICROCIRCUITS LTD

PRODUCT INFORMATION

Obsolete Product
- For Information Only -

D/244/2/020



FX403-Q

QTC ADDRESS & DATA ENCODER DECODER

* N-DIGIT HSC ADDRESS DECODING
* GROUP AND ALL-CALL DECODING
* EXPANDABLE CODE-ROM ADDRESSING
* LOW POWER CMOS PROCESS
* DECODES SUFFIX INSTRUCTION CODES
* CODED BLEEP AND AUDIO MUTE OUTPUTS
* ENCODES N-DIGIT ADDRESS/DATA CODES
* TRANSMIT/TRANSPOND ENCODE FUNCTIONS

The FX403Q is an address/decoder/encoder operating in accordance with the HSC rules. It is intended for use in mobile, portable and fixed station tone operated selective signalling applications. In decode mode, it accepts 4 bit QTC data characters from an FX-003 tone decoder and compares these with an address held in an external memory (ROM). Receipt of a correct code causes the $\overline{\text{MUTE}}$ output to switch and an alert pattern to be output at the AUDIO output. The alert tone is a 2.121kHz square wave, interrupted in a set pattern governed by the type of information decoded (eg. address, address and data, group call). These audible warnings are output continuously until reset.

Further decoding of an address can be stopped if failure to meet any timing or HSC format requirement is detected. It decodes valid group codes and a series of address suffix codes as defined in HSC. These include instructions to inhibit alerts mute audio and inhibit/initiate transpond. Where a valid address or group code is followed by a data sequence, a DATA FLAG is set and a LOAD PULSE for each character of data is output. The FX403Q can be instructed to automatically transpond an address or sequence stored in the external memory.

When used with an FX503 it will perform encoding functions to generate address and data codes. Address codes can be held in an external memory and loaded under instruction into the FX503 for generation. Uses nominal 5V supply.

PIN CONNECTIONS FX403-Q

1. Data change	28. D_3 Data Inputs
2. Power Up Reset(PURS)	27. D_2 " "
3. V_{ss}	26. D_1 " "
4. Audio Reset	25. D_0 " "
5. $\overline{\text{Decode Invalid}}$	24. Data Flag
6. Transpond Mode	23. V_{dd}
7. Audio Output	22. $\overline{\text{Mute}}$ Reset
8. Clock	21. $\overline{\text{Mute}}$
9. Increment Address	20. TX Enable
10. Load Pulse	19. TX Relay
11. Q_{po} Outputs to Address ROM	18. D_{p3} Inputs from ROM
12. Q_{p1} " " " "	17. D_{p2} "
13. Q_{p2} " " " "	16. D_{p1} "
14. Q_{p3} " " " "	15. D_{p0} "

PIN NUMBER	FUNCTION
1	DATA CHANGE - this information comes from the FX003 and is a short positive pulse indicating that a change of character has been detected.
2	POWER UP RESET (PURS) - initially when the power is applied, the circuit will reset itself into the receive mode of operation with the audio muted. The reset sequence is initiated by a logical "1" on the PURS input for a minimum period of 80µS. This can be achieved by the use of an RC network on this input.
3	VSS -
4	AUDIO RESET - this pin is an I/O port. The input function is activated by applying a logical "1" pulse to the pin of sufficiently low impedance (typically a switch) to overcome the internal pull-down transistor. The internal pull-down transistor is disabled under certain circumstances to facilitate the use of an external RC network to automatically reset the audio output after a user-determined time. The two conditions which disable the internal pull-down transistor are when either a group call or address call without data but requesting transpond, have been received. By applying a logical "1" to the AUDIO RESET input, when the device is outputting a data alert (address & data) the AUDIO output and the $\overline{\text{MUTE}}$ output will be reset.
5	$\overline{\text{DECODE INVALID}}$ - the input is inoperative when held at logical "1" and active when at logical "0". It is enabled only whilst decoding an address sequence and not during the decoding of flag tones or during a transmit or transpond routine it does not reset the $\overline{\text{MUTE}}$ output AUDIO output, TRANSMIT ENABLE or RELAY outputs.

6 TRANSPOND MODE - this input can be used to initiate a transpond action upon receipt of a valid address. For this purpose the input must be at a logical "1". If a group address is received whilst this mode had been selected, then the circuit will over-ride the transpond request but otherwise function normally. Transponding sequences are completed before any audio alert patterns are output. Previous alert patterns are then reset.

A transpond will only be initiated if:

(i) A transpond has been selected.

(ii) The decoded valid address did not contain a Group tone.

(iii) The device has received hex code "F" (NOTONE) to signify that no transmissions are in progress.

7 AUDIO OUTPUT - the various alert patterns are output from this pin. The output impedance is 3KΩ.

8 CLOCK - A 23.3kHz clock should be used

9,10 INCREMENT ADDRESS/LOAD PULSE - the INCREMENT ADDRESS input and LOAD PULSE output are enabled when the RELAY output is at logical "1". The Schmitt trigger input is activated by a logical "1" pulse of minimum duration 1mS. The "Address outputs" will increment by 1 count 40-470µS after the input exceeds the Schmitt trigger logical "1" level and 470µS after that a 40µS logical "1" pulse will be generated at the LOAD PULSE output.

No further action will be taken until after the input returns to logical 0, after which it can once more initiate the sequence.

11,12,13,14 ADDRESS OUTPUTS (Q_{po}-Q_{p3}) - the external memory is addressed by four address output lines (Q_{po}-Q_{p3}) which increment as a binary count. The address outputs reset to address the first ROM location (0001) in the receive or transmit mode. If transpond mode is selected then address outputs move on to location 9 (1001) for start of transpond address. The outputs are reset when hex-code "F" is detected.

15,16,17,18 INPUTS FROM 'ROM'.

19 RELAY OUTPUT - Quiescent state is at logical "0". Output changes to logical "1" when either a transpond request or transmit command has been received.

This is true only if the circuit is not in the process of decoding an address or data package. The output is reset when the 'memory' inputs hex-code 'E'.

20 TRANSMIT ENABLE (TX) - this pin is an I/O port. It can be activated by an A.C. coupled logical "1" pulse of 40µS duration. The circuit will only begin to activate a transmit command when:

(i) the circuit is not in the process of decoding an address or data package i.e. input is Hex Code "F".

(ii) the RELAY output is not activated.

When a pulse is activated at the TRANSMIT ENABLE the device latches the command and outputs a logical "1". When a transmit command is accepted the AUDIO output is reset if it is operated. The output is reset when the memory inputs hex code "E".

21,22 $\overline{\text{MUTE}}/\overline{\text{MUTE}}$ RESET - By means of a $\overline{\text{MUTE}}$ output the device may control the unmuting of an audio stage. The quiescent state (muted) is with the output at VSS (Logical 0). The MUTE RESET i/p can be used to reapply the MUTE. The quiescent state is with the $\overline{\text{MUTE}}$ RESET input at logical "0". Applying a logical "1" to the AUDIO RESET input when the device is outputting a data alert pattern will reset both the AUDIO output and the $\overline{\text{MUTE}}$ output.

23 VDD

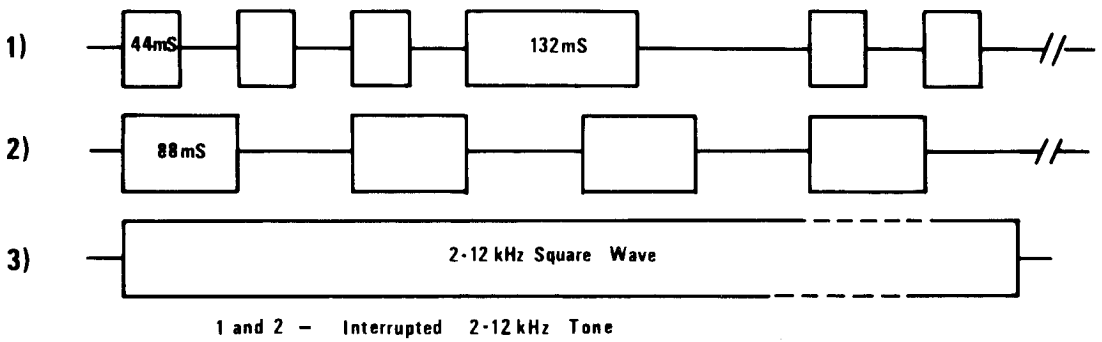
24 DATA FLAG - output is activated after receipt of a correct address followed by flag tone "B". The output will change to logical "1" just after the leading edge of the data change pulse associated with the "B" tone (typically 40µS) and will change back to logical "0" shortly after the leading edge of the data change pulse associated with the next "F" tone. All tones after flag tone "B" are regarded by the circuit as a data package. A logical "1" pulse of 40µS is output for each data character from the LOAD PULSE output.

When DATA FLAG is connected to LOAD ENABLE of the FX303, the data following after the address can be loaded into the FX303 for subsequent display.

25,26,27,28 DATA INPUTS - 4 bit data inputs come from FX003 Tone Decoder. They represent all digits, suffix codes, group and repeat codes and data.

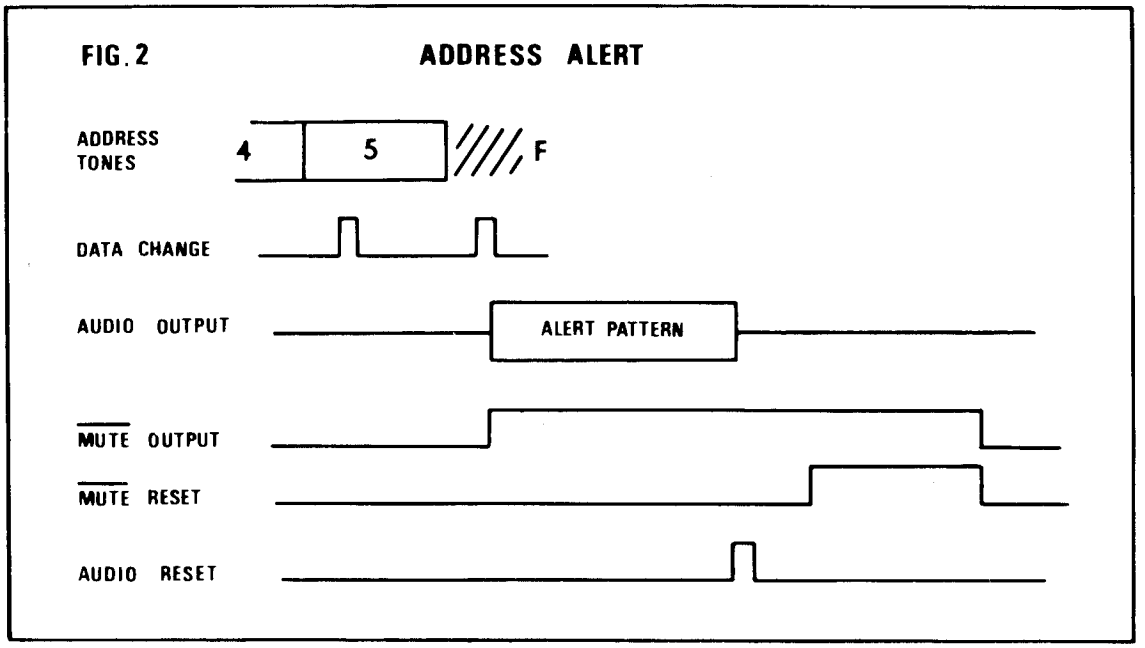
FIG.1 AUDIO ALERT TONE PATTERNS

INFORMATION DECODED	**PATTERN**
1) Address and Data	**'V' Pattern**
2) Address	**Equal Mark Space Ratio**
3) Group Address	**Continuous Tone**



1 and 2 – Interrupted 2·12 kHz Tone

An audio bleep pattern is generated to indicate that a valid address has been decoded. The continuous tone is a 2.12lkHz square wave. This is interrupted in audibly recognisable patterns depending upon what information has been decoded. The bleep pattern will be generated continuously until reset by either the AUDIO RESET input or the $\overline{\text{MUTE}}$ RESET input.



PROGRAMMING THE EXTERNAL MEMORY

The first 8 locations of the external memory are reserved for receiving and transmit codes. An address is "written" into these locations and compared with a received code, to verify a valid address call.

Transpond codes should be "written" into the ROM after location 8 and terminated with flag tone E. Codes up to 7 digits in length are permissable and must be terminated with flag tone E.

When programming the ROM, flag tone E should not be used to indicate repeat of a digit. The memory should be programmed as written.

eg. (i) Address Code 12345
- should be "written" as 12345E.

(ii) Address Code 12234
- should be "written" as 12234E.

In transpond mode the FX403 will automatically step to the 9th memory location and transmit the code stored there. If a transpond action is required the FX403 should be connected to the FX503 (QTC/XTC Tone Generator) as shown in Fig.(5).

A transpond code should be programmed, beginning at address 9 and being followed immediately by hex-code E.

Example:

External Memory Locations 5 6 7 8 9 10 11 12 13 E

Transpond Code

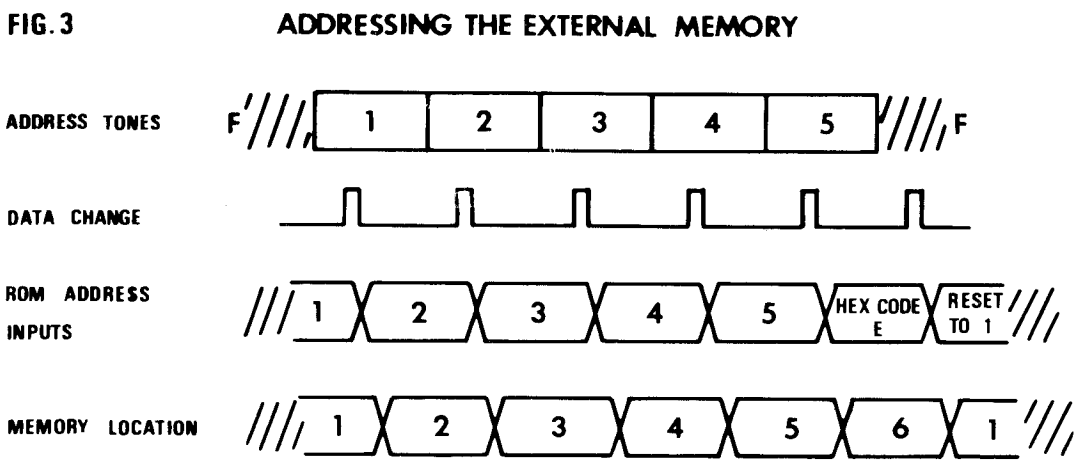
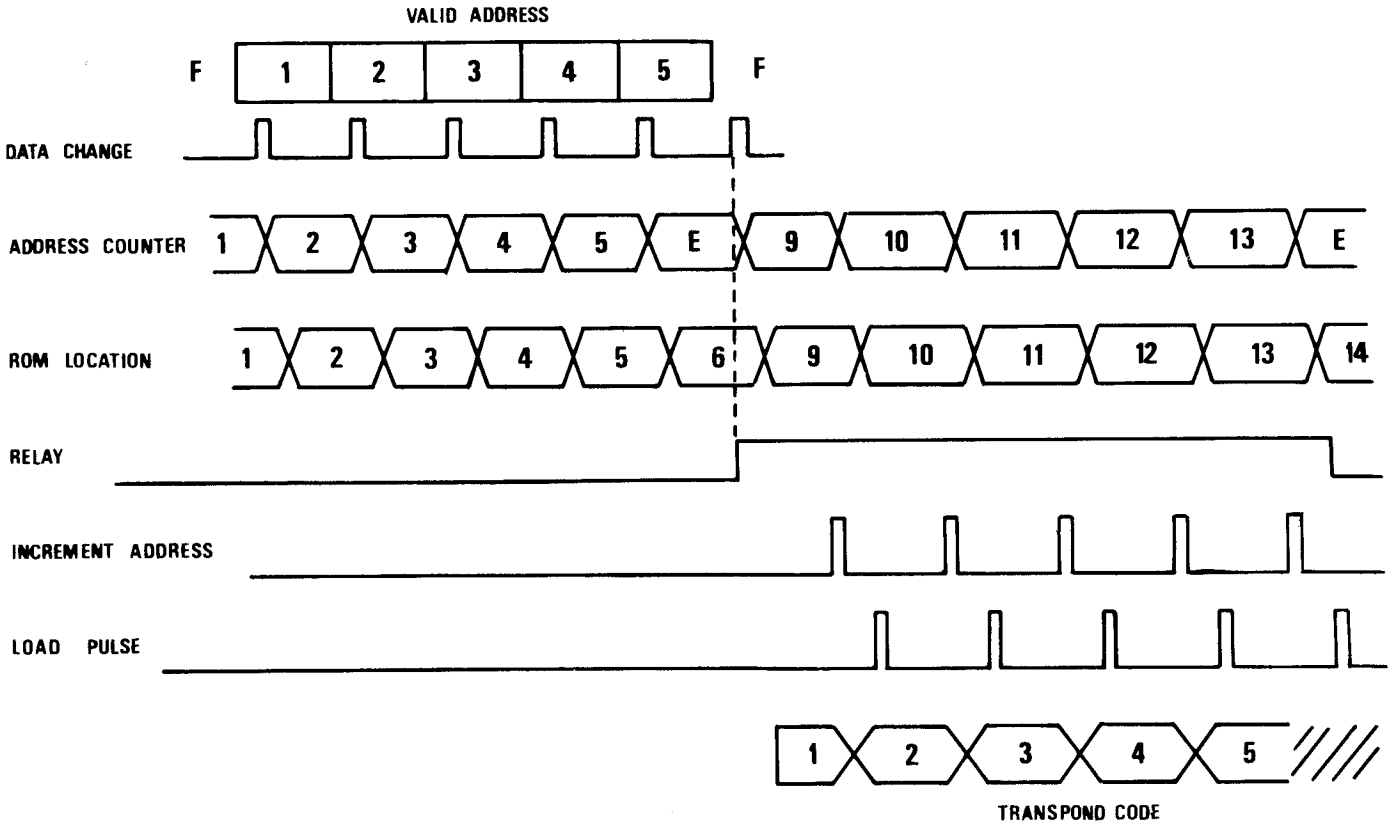


FIG.4 ACTION TAKEN IN TRANSPOND MODE



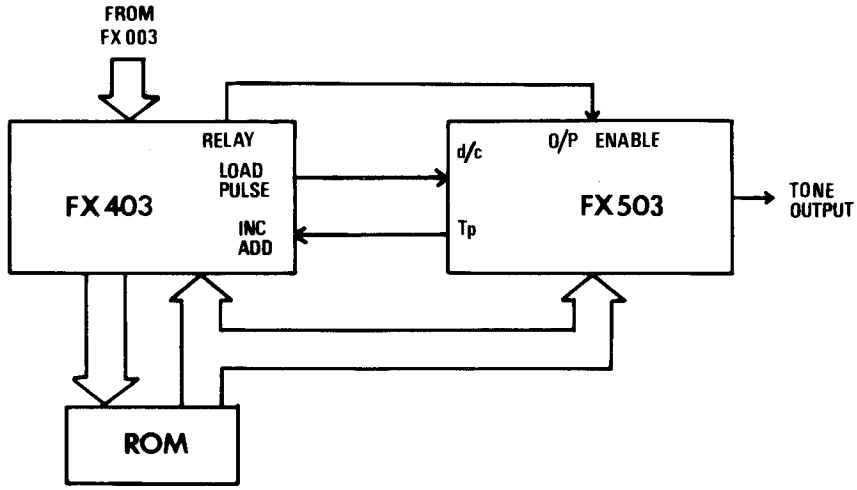


FIG. 5 TRANSPOND ARRANGEMENT