Consumer Microcircuits Limited

PRODUCT INFORMATION

FX326 AUDIO BANDPASS FILTER

With compliments of Island Labs

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PROVISIONAL ISSUE

Features

- 300 – 3000/3400Hz Audio Bandpass Filter
- Low Group Delay Distortion
- On-Chip Uncommitted Amplifier
- Switched Capacitor Filters
- Choice of Xtal/Resonator Frequencies
- Chip Enable Powersave Feature
- Single 5V CMOS Process
- Surface Mounted or DIL Package

Applications

- Alarm Systems
- Portable Audio Equipments
- Data Signalling—Modems
- PABX and Trunk Equipment
- Cordless Telephones and Intercoms
- Mobile Radio Audio Processing
- Delta Modulation Audio Filtering
- Medical Instrumentation
- Automotive Products

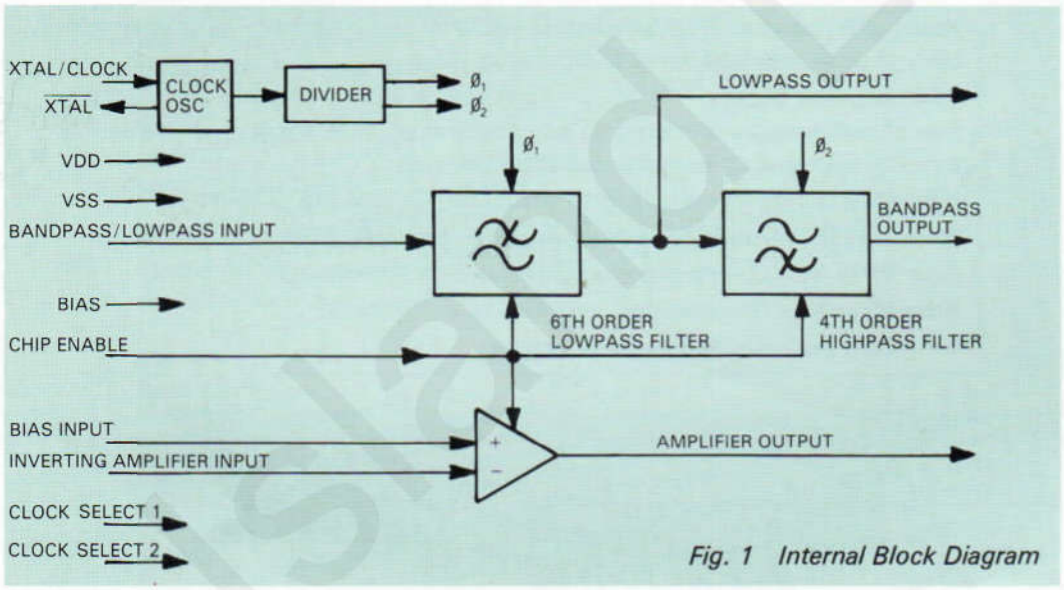


Fig. 1 Internal Block Diagram

FX326

Brief Description

The FX326 is a general purpose low power CMOS switched capacitor audio bandpass filter. The filter frequency response is clock related; however, the programmable divider allows for a standard 300 – 3000Hz or 300 – 3400Hz frequency response (see Fig. 3). The device in detail consists of:

(1) a 6th order low group delay distortion lowpass filter
(2) a 4th order highpass filter
(3) an uncommitted amplifier

The two filters are connected in series, thus providing an audio bandpass filter; however, the lowpass filter may be used independently.

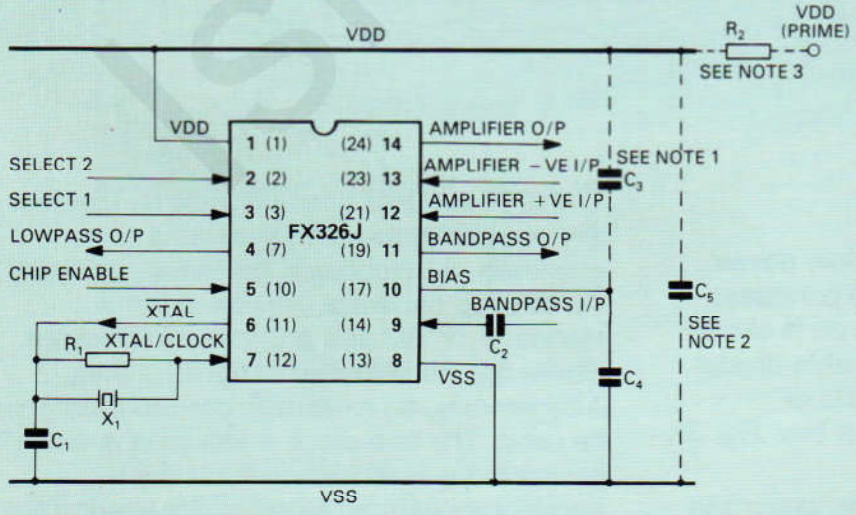
The uncommitted amplifier may be used for any specific application such as pre-emphasis, de-emphasis, buffering, gain, etc. An on-chip oscillator uses an external resonator or xtal and provides all reference clocks for the switched capacitor filters. Alternatively, an externally derived clock may be used. The two clock select lines enable the device to be used with various clock frequencies without significantly altering the filter response. Alternatively, re-programming of the clock select lines, or varying the clock frequency, will shift the filter cutoff frequencies (see Fig. 3). The chip enable input is used to disable the filter and amplifier sections, thus reducing current consumption.

Pin Number — Function

FX326J	FX326LV1	Function
1	1	**VDD:** Positive Supply.
2	2	**Select 2:)** Inputs to on chip programmable divider used to select required
3	3	**Select 1:)** operating xtal/clock frequency. Both pins have 1MΩ internal pull down resistors (see Fig. 3). The upper and lower cutoff frequencies are controlled by the clock frequency ϕ, division ratio n and a design constant.
		The typical lower cutoff frequency f_L is given by: $f_L = \frac{2.5\,\phi}{n}$ where f_L is −3dB frequency in Hz; ϕ is clock frequency in kHz; n is set by S1, S2.
		The corresponding upper cutoff frequency f_H is given by $f_H = \frac{34\,\phi}{n}$
		The relationship between S1, S2 and n is:

S1	S2	n
0	0	10
0	1	6
1	0	20
1	1	12

4	7	**Lowpass O/P:** This is the output of the lowpass filter section and is internally biased to VDD/2.
5	10	**Chip Enable:** Internally pulled to VDD. A logic '0' applied to this input will disable all filters and the uncommitted amplifier. (Powersave).
6	11	**Xtal:** Xtal output. Inverting output of on chip oscillator.
7	12	**Xtal/Clock:** Input to on-chip inverting oscillator. Xtal resonator input or externally derived clock may be applied to this input.
8	13	**VSS:** Negative Supply.
9	14	**Bandpass/Lowpass I/P:** Input to lowpass filter which is connected in series with the Highpass filter to form the Bandpass section.
10	17	**Bias:** VDD/2 Bias pin externally decoupled by C_4 (see Fig. 2, Note 1).
11	19	**Bandpass O/P:** Output from Highpass filter, internally biased to VDD/2.
12	21	**Amp I/P (+VE):** Uncommitted amplifier, non-inverting input.
13	23	**Amp I/P (−VE):** Uncommitted amplifier, inverting input.
14	24	**Amp O/P:** Uncommitted amplifier output.



(FX326LV1 SHOWN IN BRACKETS. NO CONNECTION PINS: 4, 5, 6, 8, 9, 15, 16, 18, 20, 22)

Fig. 2 External Component Connections

Component References

Component	Unit Value	Tolerance
R_1	1M	± 10%
R_2	—	(See note 3)
C_1	33p	± 20%
C_2	0.1μ	(See note 1)
C_3	0.1μ	(See note 1)
C_4	0.1 μ	(see Note 1)
C_5	—	(See notes 2, 3)
X_1	Crystal	

NOTES:

1. *Bias may be decoupled to VSS and VDD using C_3, C_4 when input signals are referenced to the bias pin. For input signals referenced to VSS, decouple Bias to VSS using C_4 only.*
2. *Use C_5, when input signals are referenced to VSS, to decouple VDD.*
3. *Use R_2 to assist decoupling of high frequency power supply noise (R_2 C_5 typically 300μs)*

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)		−0.3V to (VDD + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX326J	−30°C to + 85°C
	FX326LV1	−30°C to + 70°C
Storage temperature range:	FX326J	−55°C to +125°C
	FX326LV1	−40°C to + 85°C
Maximum device dissipation		All versions 100mW

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
VDD = 5V, T_{amb} = 25°C, ϕ = 1MHz, (pin 2 and pin 3 open circuit), Δf_{ϕ} = 0, f_{in} = 1kHz, 100 mV rms.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5	5.5	V
Supply current (Enabled)		—	3.5	—	mA
Supply current (Disabled)		—	1	2	mA
Input impedance (Filters & Amplifier)		100	—	—	kΩ
Output impedance (Filters)		—	3	—	kΩ
Output impedance (Amplifier open loop)		—	800	—	Ω
Output impedance (Amplifier closed loop)		—	6	—	Ω
Input logic '1'		3.5	—	—	V
Input logic '0'		—	—	1.5	V
On-chip crystal oscillator: R in		10	—	—	MΩ
R out		5	—	15	kΩ
Inverter gain		10	—	20	dB
Gain Bandwidth Product		3	—	—	MHz
Crystal/Resonator Frequency	1		1		MHz
Dynamic Characteristics					
Passband Ripple (400 — 2800Hz)		—	—	2	dB
Cutoff Frequency LP (−3dB)		—	3400	—	Hz
HP (−3dB)		—	260	—	Hz
Stopband Attenuation (f> 6kHz)		—	35	—	dB
(f< 200Hz)		—	15	—	dB
Output Noise (rms)	2	—	1.6	—	mV
Signal Input Range (rms)	3	—	0.4	1.0	V
Insertion Loss (1kHz)			0		dB
Aliasing Frequency		$\frac{\phi}{2n}$			Hz
Uncommitted Amplifier					
Open loop gain	4	—	30	—	dB
Gain BW Product		—	1	—	MHz

Notes:

1). For other frequencies see Fig. 3.
2). Measured with input ac short circuit
3). 'MAX' figure specified for nominal 3% distortion (30dB SINAD).
'TYP' figure specified for minimum distortion (MAX SINAD).
4). Relative to 1kHz, 100 mV rms input level.

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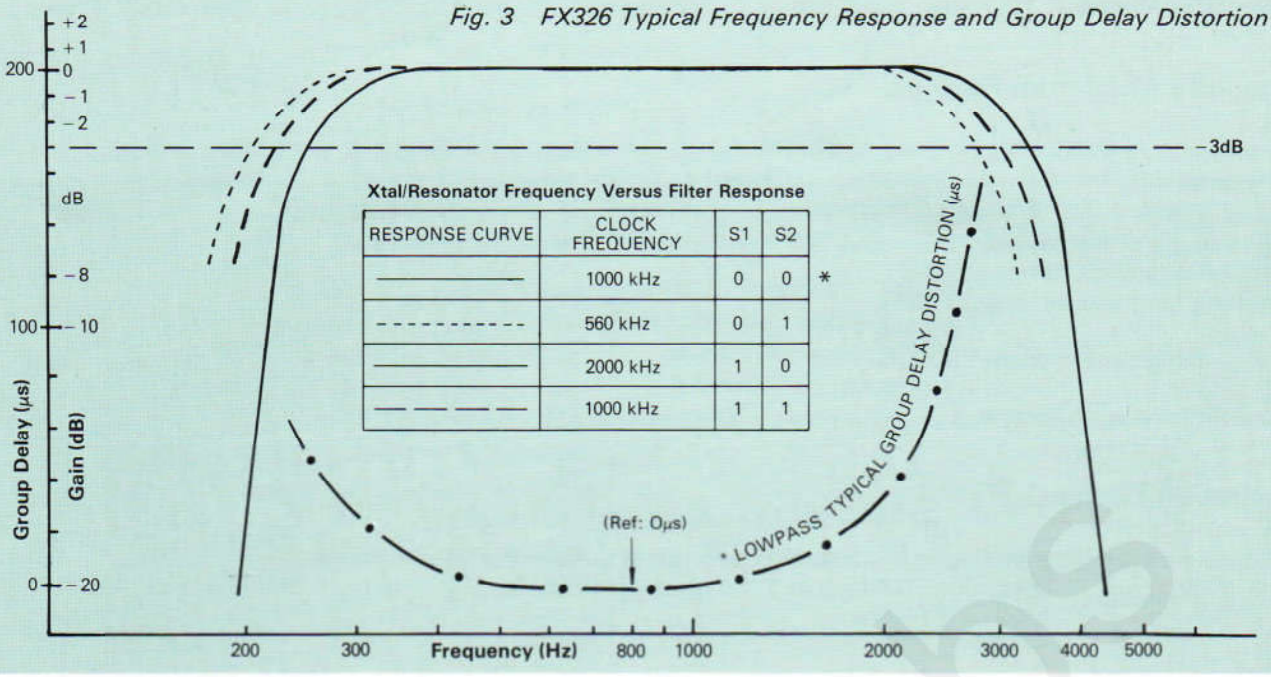
Fig. 3 FX326 Typical Frequency Response and Group Delay Distortion



Xtal/Resonator Frequency Versus Filter Response

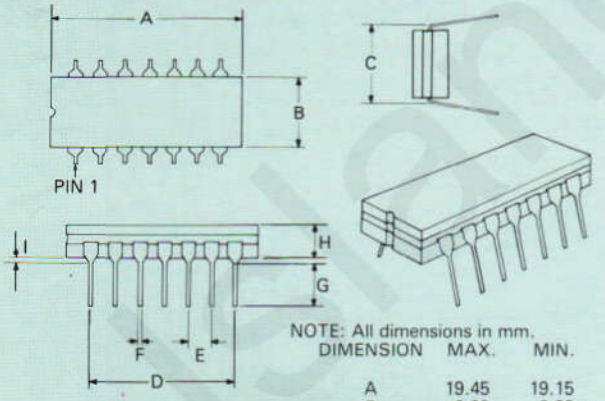
RESPONSE CURVE	CLOCK FREQUENCY	S1	S2	
———	1000 kHz	0	0	*
- - - - - - - - - -	560 kHz	0	1	
———	2000 kHz	1	0	
— — — —	1000 kHz	1	1	

Package Outlines

The cerdip package of the FX326J is shown in *Figure 4.* The FX326LV1 of *Figure 5* is supplied in a conductive tray.

The FX326LV1 has an indent (spot) adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 to allow complete identification. Pins number counter-clockwise when viewed from the top (indent side).

Fig. 4 ***FX326J*** *D.I.L. Package*



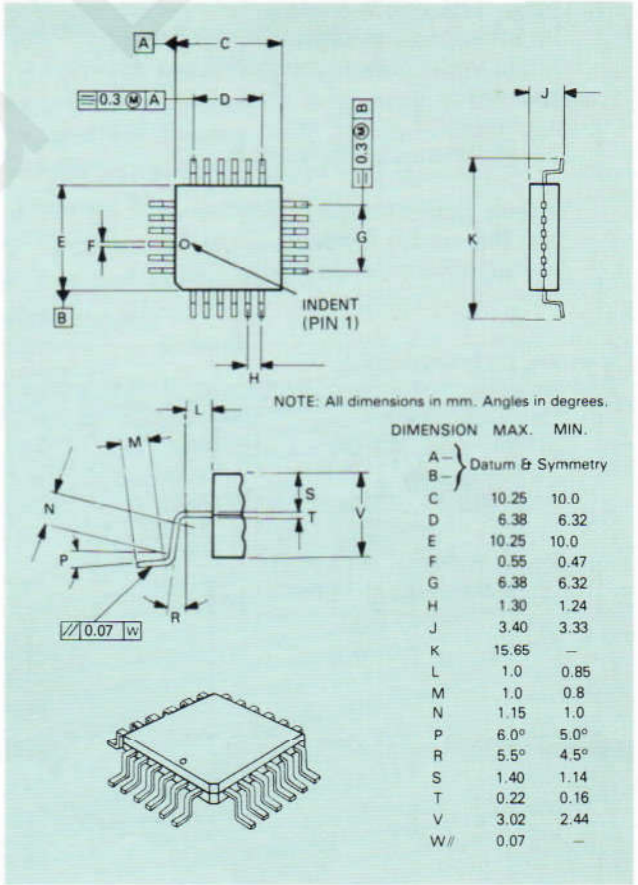
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.	
A	19.45	19.15	
B	6.38	6.22	
C	8.00	7.75	
D	15.34	15.14	
E	2.54		Typical
F	0.46		Dimension
G	4.35		
H	2.04	1.78	
I	—	0.5	

Handling Precautions

The FX326J/LV1 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

Fig. 5 ***FX326LV1*** *Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.	
A			Datum & Symmetry
B			
C	10.25	10.0	
D	6.38	6.32	
E	10.25	10.0	
F	0.55	0.47	
G	6.38	6.32	
H	1.30	1.24	
J	3.40	3.33	
K	15.65	—	
L	1.0	0.85	
M	1.0	0.8	
N	1.15	1.0	
P	6.0°	5.0°	
R	5.5°	4.5°	
S	1.40	1.14	
T	0.22	0.16	
V	3.02	2.44	
W//	0.07	—	

Ordering Information

FX326J **14-pin Cerdip D.I.L.**

FX326LV1 **24-pin quad plastic encapsulated, bent and cropped.**

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.

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