UHF push-pull power MOS transistor BLF548

FEATURES

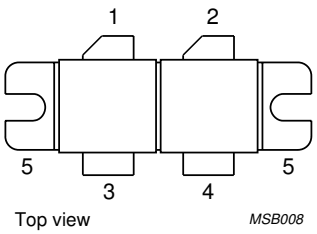
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PIN CONFIGURATION



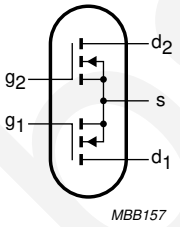


Fig.1 Simplified outline and symbol.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	150	>10	>50

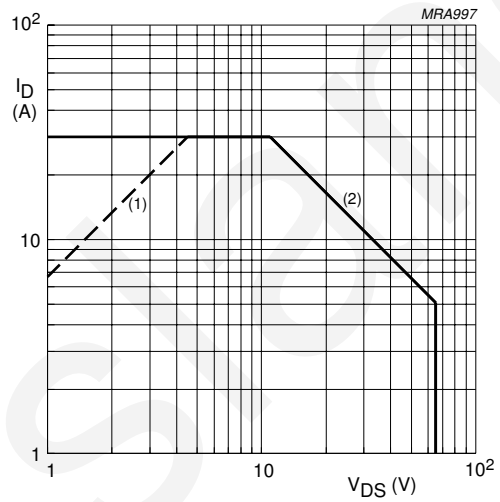
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	15	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; total device; both sections equally loaded	–	330	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

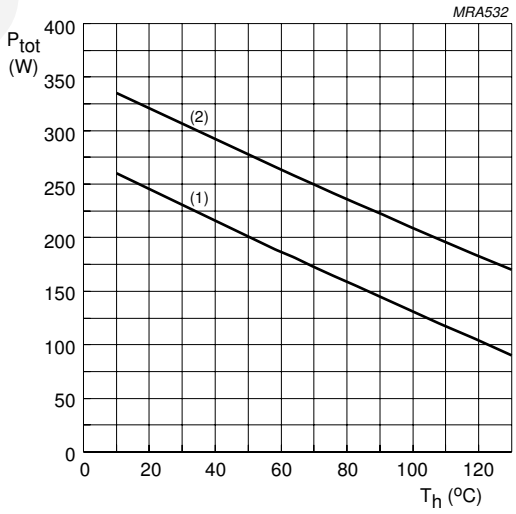
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 330 W; total device; both sections equally loaded	0.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power derating curves.

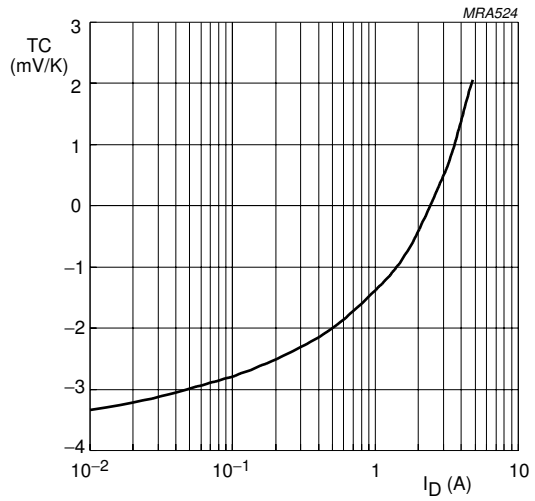
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 40 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 160 mA; V_{DS} = 10 V	2	–	4	V
g_{fs}	forward transconductance	I_D = 4.8 A; V_{DS} = 10 V	2.4	3.5	–	S
R_{DSon}	drain-source on-state resistance	I_D = 4.8 A; V_{GS} = 10 V	–	0.25	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	16	20	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	105	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	90	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF

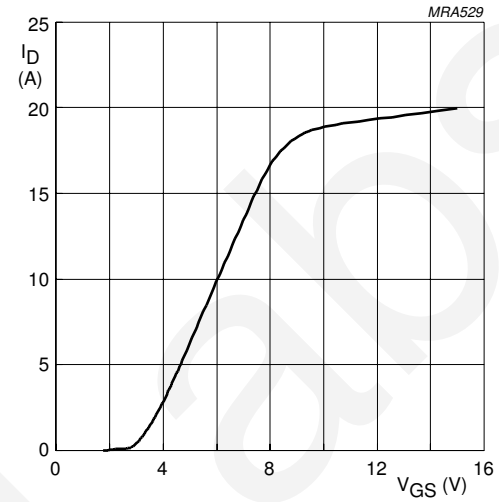
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



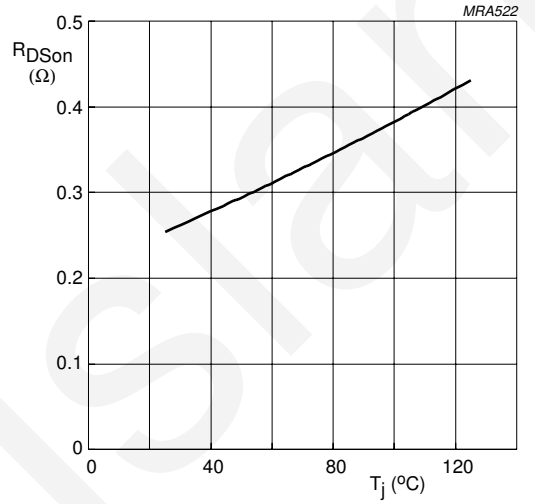
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



I_D = 4.8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.

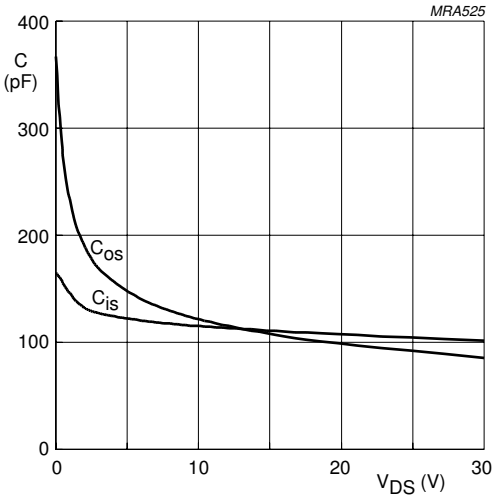


Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.

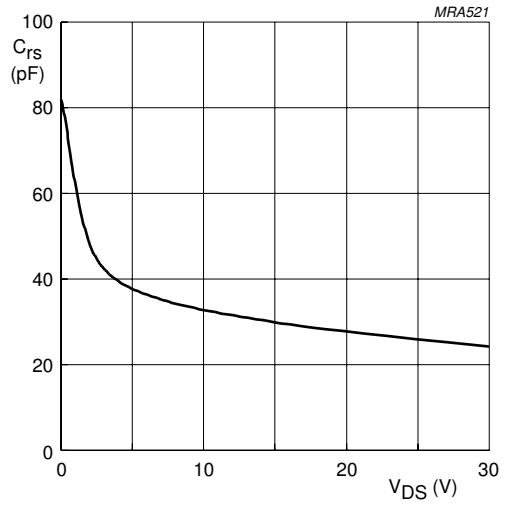


Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

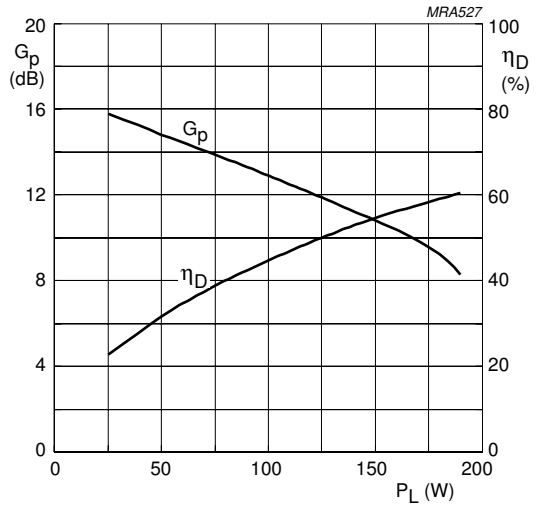
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.

RF performance in a common source, class-B, push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 160	150	>10 typ. 11	>50 typ. 55

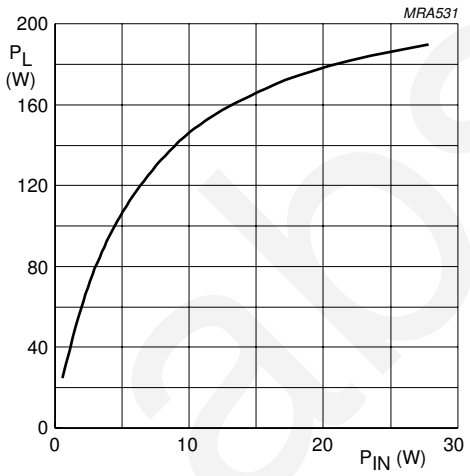
Ruggedness in class-B operation

The BLF548 is capable of withstanding a load mismatch corresponding to VSWR = 10: 1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



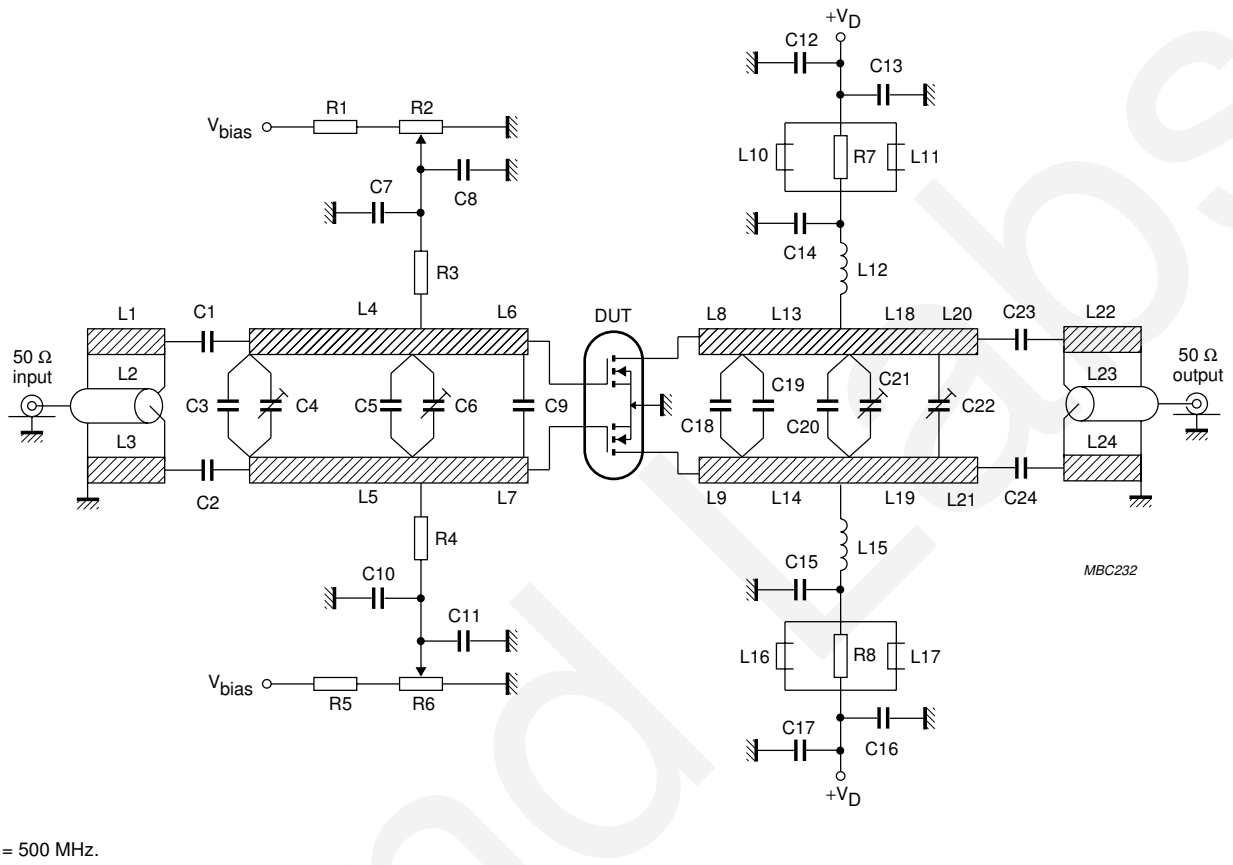
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power; typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.10 Load power as a function of input power; typical values.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

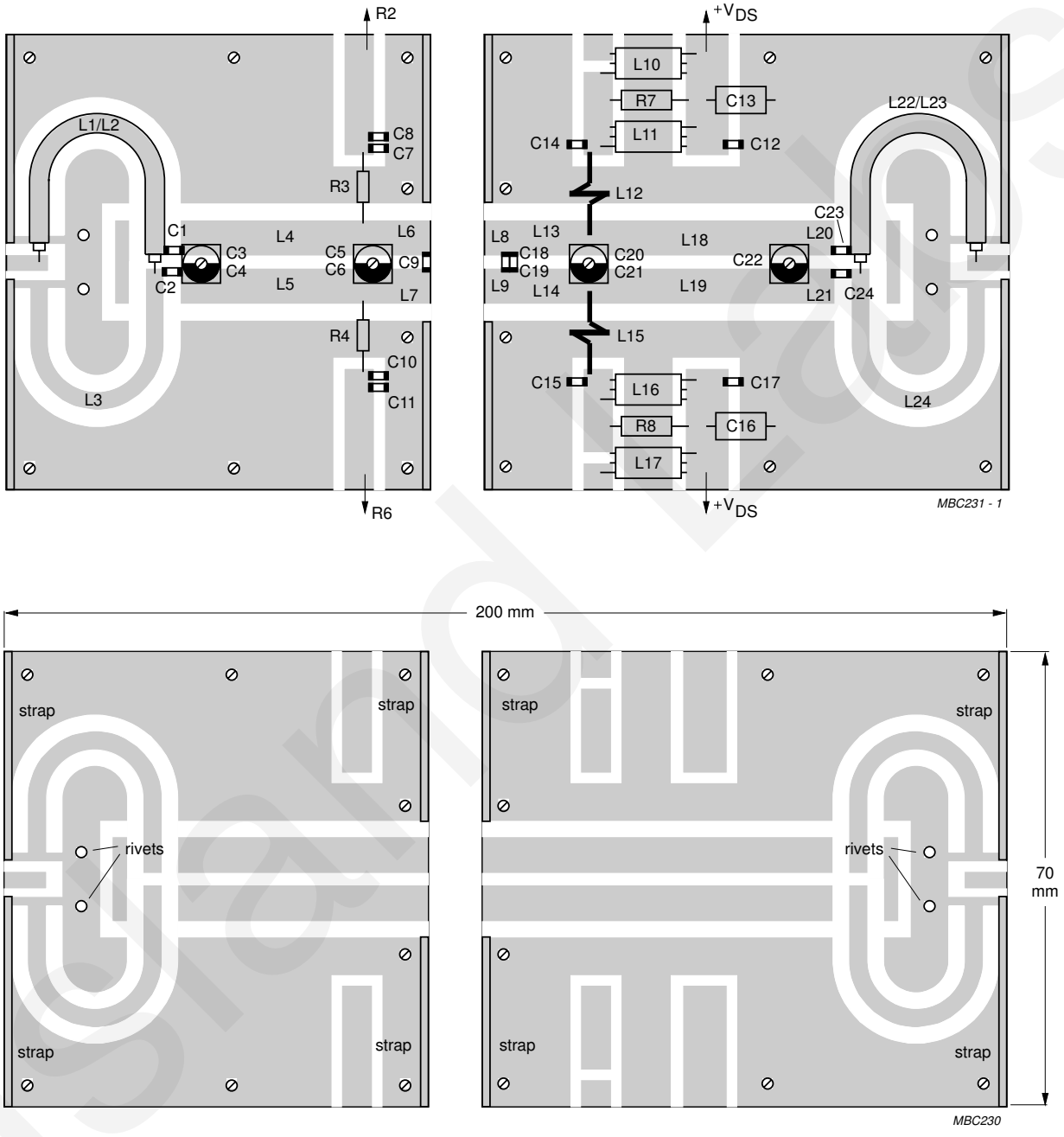
List of components class-B test circuit (see Fig.11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	22 pF		
C3	multilayer ceramic chip capacitor; note 1	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor; note 2	27 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor; note 1	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor; note 3	2×56 pF in series		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C13, C16	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C18	multilayer ceramic chip capacitor; note 2	18 pF		
C19	multilayer ceramic chip capacitor; note 2	12 pF		
C20	multilayer ceramic chip capacitor; note 2	8.2 pF		
C23, C24	multilayer ceramic chip capacitor; note 1	30 pF		
L1, L3, L22, L24	stripline; note 4	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable; note 5	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline; note 4	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline; note 4	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline; note 4	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 × 5 mm	
L13, L14	stripline; note 4	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline; note 4	22.3 Ω	length 36 mm width 7 mm	
L20, L21	stripline; note 4	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 kΩ		2322 151 72473
R2, R6	10 turn potentiometer	5 kΩ		
R3, R4	0.4 W metal film resistor	10.5 kΩ		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 51009

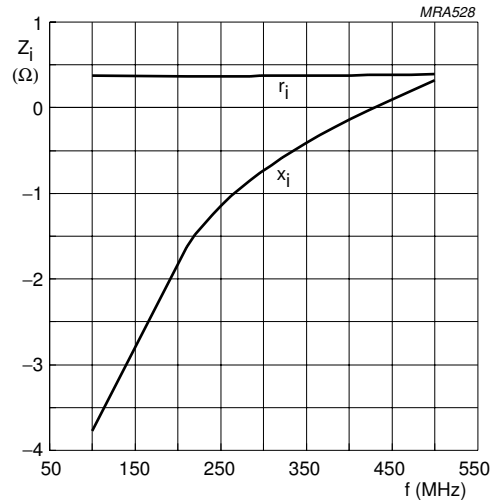
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed-circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 0.79 mm.
5. Cables L2 and L23 are soldered to striplines L1 and L22 respectively.



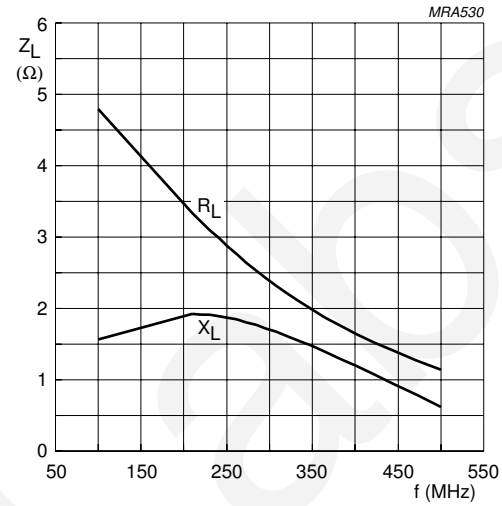
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.13 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.14 Load impedance as a function of frequency (series components); typical values per section.

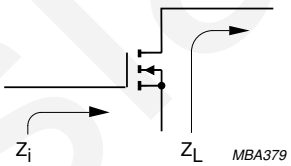
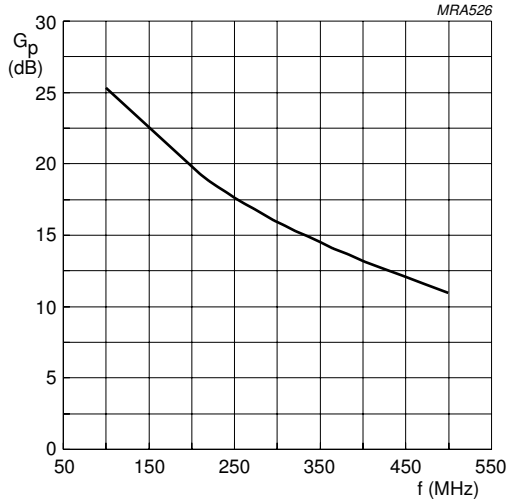


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.16 Power gain as a function of frequency; typical values per section.

BLF548 scattering parameters

V_{DS} = 28 V; I_D = 40 mA; note 1

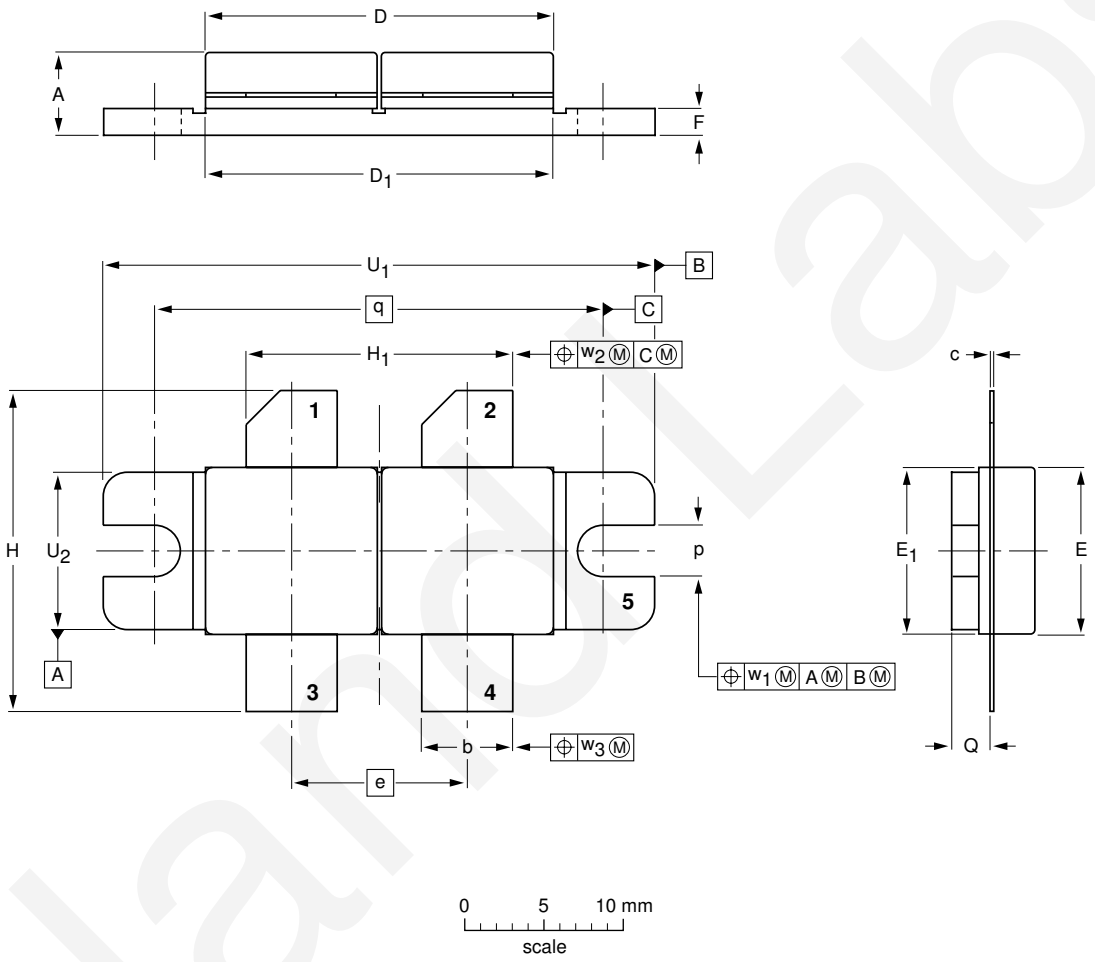
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	$\angle\Phi$	$\|s_{21}\|$	$\angle\Phi$	$\|s_{12}\|$	$\angle\Phi$	$\|s_{22}\|$	$\angle\Phi$
5	0.99	−14.0	13.60	171.0	0.02	81.0	0.89	−12.8
10	0.98	−27.6	13.20	162.0	0.04	72.4	0.87	−25.3
20	0.93	−52.0	11.90	146.0	0.07	57.1	0.82	−48.0
30	0.88	−72.0	10.30	134.0	0.09	44.8	0.77	−66.6
40	0.84	−87.7	8.93	124.0	0.10	35.2	0.72	−81.3
50	0.81	−100.0	7.75	116.0	0.11	27.7	0.68	−93.0
60	0.79	−110.0	6.78	110.0	0.12	21.6	0.66	−102.0
70	0.77	−118.0	6.00	104.0	0.12	16.7	0.64	−109.0
80	0.76	−124.0	5.36	99.8	0.12	12.5	0.63	−115.0
90	0.75	−129.0	4.82	95.9	0.12	8.9	0.62	−120.0
100	0.75	−133.0	4.37	92.3	0.13	5.7	0.61	−124.0
125	0.74	−141.0	3.53	84.7	0.13	−1.1	0.61	−131.0
150	0.74	−147.0	2.94	78.3	0.13	−6.6	0.61	−137.0
175	0.74	−151.0	2.50	72.6	0.12	−11.5	0.62	−140.0
200	0.75	−154.0	2.16	67.5	0.12	−15.8	0.64	−143.0
250	0.77	−159.0	1.67	58.4	0.12	−23.3	0.67	−148.0
300	0.78	−163.0	1.33	50.4	0.11	−29.7	0.70	−151.0
350	0.80	−167.0	1.09	43.1	0.10	−35.3	0.73	−154.0
400	0.82	−169.0	0.91	36.6	0.10	−40.3	0.75	−157.0
450	0.84	−172.0	0.77	30.6	0.09	−44.7	0.78	−160.0
500	0.85	−175.0	0.66	25.1	0.08	−48.6	0.80	−162.0
600	0.89	−179.0	0.50	15.6	0.07	−55.2	0.84	−167.0
700	0.90	177.0	0.39	7.5	0.06	−60.4	0.88	−170.0
800	0.92	173.0	0.32	0.6	0.05	−64.3	0.90	−174.0
900	0.93	169.0	0.26	−5.4	0.04	−67.3	0.92	−177.0
1000	0.94	166.0	0.22	−10.8	0.04	−69.2	0.93	−179.0

Note

1. For more extensive s-parameters see internet:
   http://www.semiconductors.philips.com/markets/communications/wirelesscommunications/broadcast

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A2						99-03-29

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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